

# iC-MU OFF-AXIS NONIUS ENCODER WITH INTEGRATED HALL SENSORS

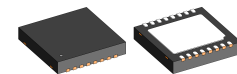
## FEATURES

Integrated Hall sensors for two-track scanning  
 Hall sensors optimized for 1.28 mm pole width (master track)  
 Signal conditioning for offset, amplitude, and phase  
 Sine/digital real-time conversion with 12-bit resolution (14-bit filtered)  
 2-track nonius absolute value calculation up to 18 bits  
 16, 32, or 64 pole pairs per measurement distance  
 Enlargement of measurement distance with second iC-MU  
 Synchronization of external multitrans systems  
 Configuration from an external EEPROM using a multimaster I2C interface  
 Microcontroller-compatible serial interface (SPI, BiSS, SSI)  
 Incremental quadrature signals with an index (ABZ)  
 FlexCount<sup>®</sup>: scalable resolution from 1 up to 65536 CPR  
 Commutation signals for motors from 1 up to 16 pole pairs (UVW)

## APPLICATIONS

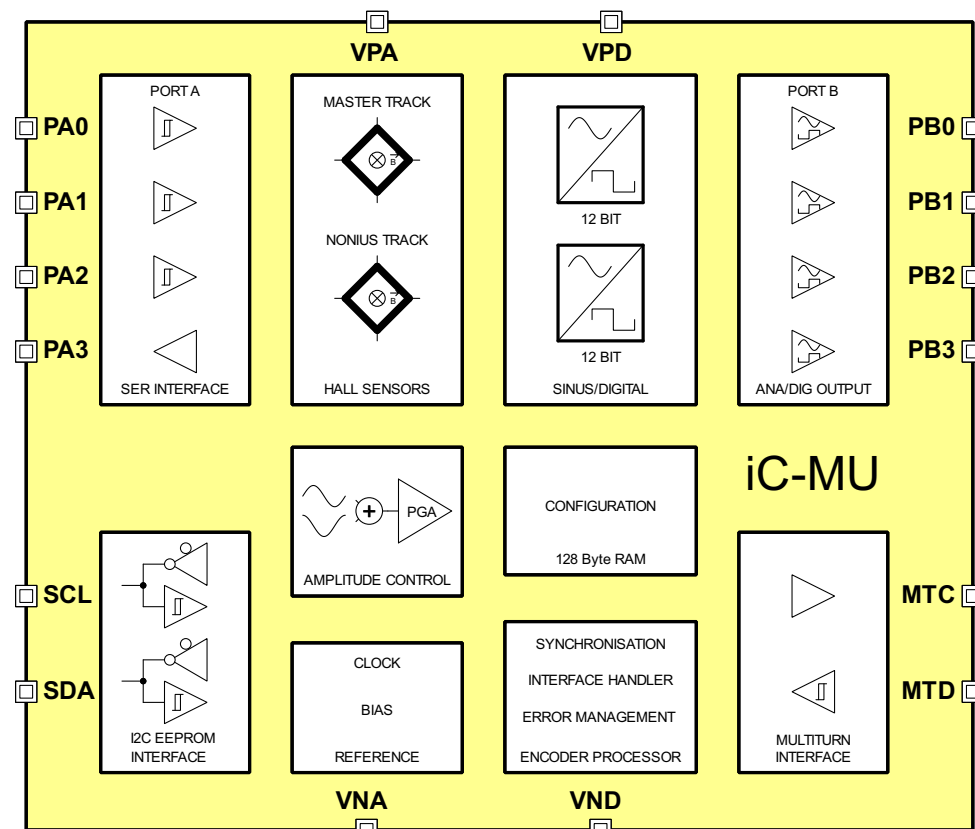
Rotative absolute encoders  
 Linear absolute scales  
 Singleturn and multitrans encoders  
 Motor feedback encoders  
 BLDC motor commutation  
 Hollow shaft encoder  
 Multi-axis measurement systems

## PACKAGES



DFN16  
5 mm x 5 mm

## BLOCK DIAGRAM



# iC-MU OFF-AXIS NONIUS ENCODER WITH INTEGRATED HALL SENSORS

preliminary



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## DESCRIPTION

iC-MU is used for magnetic off-axis position definition with integrated Hall sensors. By scanning two separate channels i.e. the master and nonius track the device can log an absolute position within one mechanical revolution. The chip conditions the sensor signals and compensates for typical signal errors.

The internal 12-bit sine/digital converters generate two position words that supply high-precision position data within one sine-period. The integrated nonius calculation engine calculates the absolute position within one mechanical revolution and synchronizes this with the master track position word. Position data can be transmitted serially, incrementally, or analog through two ports in various modes of operation. Commutation signals for brushless DC (BLDC) motors with up to 16 pole pairs are derived from the

absolute position and supplied through a 3-pin interface.

During startup the device loads a CRC-protected configuration from an external EEPROM.

After the device has been reset an optional external multiturn is read in an synchronized with the internal position data. During operation the position is cyclically checked.

The device offered here is a multifunctional iC that contains integrated BiSS C interface components. The BiSS C process is protected by patent DE 10310622 B4 owned by iC-Haus GmbH. Users benefit from the open BiSS C protocol with a free license which is necessary when using the BiSS C protocol in conjunction with this iC.

**Download the license at**  
[www.biss-interface.com/bua](http://www.biss-interface.com/bua)

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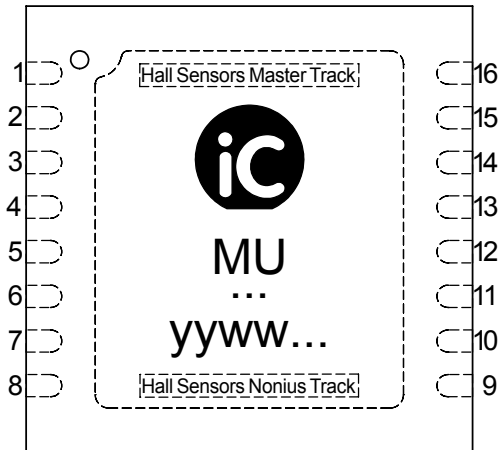
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## PACKAGING INFORMATION

### PIN CONFIGURATION



### PIN FUNCTIONS

#### No. Name Function

1	SCL	EEPROM interface, clock
2	SDA	EEPROM interface, data
3	VPA	+4.5 V... +5.5 V analog supply voltage
4	VNA	Analog Ground
5	PB0	Port B, Pin 0: Digital I/O, analog output
6	PB1	Port B, Pin 1: Digital I/O, analog output
7	PB2	Port B, Pin 2: Digital I/O, analog output
8	PB3	Port B, Pin 3: Digital I/O, analog output
9	PA3	Port A, Pin 3: Digital I/O
10	PA2	Port A, Pin 2: Digital I/O
11	PA1	Port A, Pin 1: Digital I/O
12	PA0	Port A, Pin 0: Digital I/O
13	VND	Digital ground
14	VPD	+4.5 V... +5.5 V digital supply voltage
15	MTD	Multiturn interface, data input
16	MTC	Multiturn interface, clock output
	TP	Thermal Pad

The *Thermal Pad* on the underside of the package should be appropriately connected to VNA/VND for better heat dissipation (ground plane).

Analog and digital grounds have to be connected low ohmic on the PCB.

**Only the Pin 1 mark on the front or reverse is determinative for package orientation (© MU and code are subject to change).**

# iC-MU OFF-AXIS NONIUS ENCODER WITH INTEGRATED HALL SENSORS

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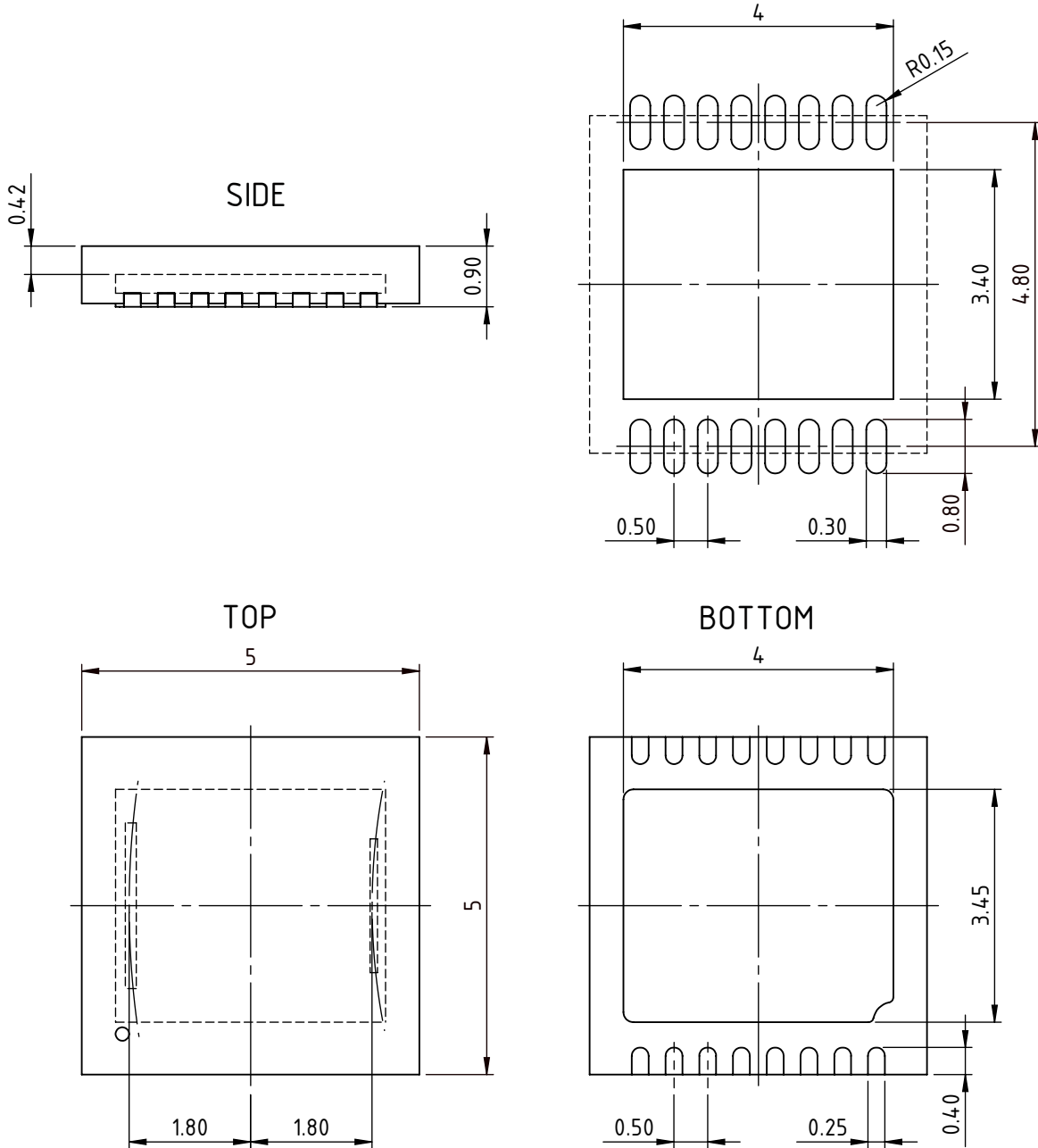


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## PACKAGE DIMENSIONS

All dimensions given in mm.

### RECOMMENDED PCB-FOOTPRINT



dra\_mu-dfn16-1\_pack\_1, 10:1

# iC-MU OFF-AXIS NONIUS ENCODER WITH INTEGRATED HALL SENSORS

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## ABSOLUTE MAXIMUM RATINGS

Maximum ratings do not constitute permissible operating conditions; functionality is not guaranteed. Exceeding the maximum ratings can damage the device

Item No.	Symbol	Parameter	Conditions	Min.		Max.		Unit
G001	V()	Voltage at VPA, VPD		-0.3		6		V
G002	I()	Current in VPA		-10		20		mA
G003	I()	Current in VPD		-10		100		mA
G004	V()	Voltage at all pins except VPD		-0.3		VPD+0.3		V
G005	I()	Current in all I/O pins	DC current Pulse width < 10 $\mu$ s	-10 -100		10 100		mA mA
G006	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 k $\Omega$			2		kV
G007	Ptot	Permissible Power Dissipation				400		mW
G008	Tj	Chip-Temperature		-40		150		$^{\circ}$ C
G009	Ts	Storage Temperature Range		-40		150		$^{\circ}$ C

## THERMAL DATA

Operating conditions: VPA = VPD = 5 V  $\pm$ 10%

Item No.	Symbol	Parameter	Conditions	Min.		Typ.		Max.		Unit
T01	Ta	Operating Ambient Temperature Range		-40				110		$^{\circ}$ C
T02	Rthja	Thermal Resistance Chip to Ambient DFN16	Surface mounted, Thermal-Pad soldered to approx. 2 cm $^2$ copper area on the PCB			40				K/W

All voltages are referenced to ground (pin VND = VNA) unless otherwise stated.

All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

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## ELECTRICAL CHARACTERISTICS

Operating conditions: VPD, VPA = 5 V ±10%, Tj = -40...125°C, IBP calibrated to 200 µA, reference is VNA = VND, unless otherwise stated

Item No.	Symbol	Parameter	Conditions				Unit
				Min.	Typ.	Max.	
<b>Total Device</b>							
101	V(VPA)	Permissible Supply Voltage at VPA		4.5	5	5.5	V
102	V(VPD)	Permissible Supply Voltage at VPD		4.5	5	5.5	V
103	I(VPA)	Analog Supply Current in VPA		3	8	12	mA
104	I(VPD)	Digital Supply Current in VPD		25	40	65	mA
105	Vc()hi	Clamp Voltage hi at all pins	Vc()hi = V() - V(VPD), I() = +1 mA	0.3		1.6	V
106	Vc()lo	Clamp Voltage lo at all pins	I() = -1 mA	-1.6		-0.3	V
107	ton()	Power-Up Time	VPD > 4 V, EEPROM Data valid		20		ms
<b>Hall Sensors</b>							
201	Hext	Operating Magnetic Field Strength	at surface of chip	15		100	kA/m
202	f()	Operating Magnetic Field Frequency				7	kHz
203	rpm	Permissible rotation of pole wheel with FRQ_CNV=lo	16 pole pairs 32 pole pairs 64 pole pairs			24000 12000 6000	rpm rpm rpm
204	vmax	Permissible movement speed				17	m/s
205	hpac	Sensor-to-Package-Surface Distance	with DFN16-5x5 mm		400		µm
<b>Assembly Tolerances</b>							
301	TOLrad	Permissible Radial Displacement				0.5	mm
302	TOLtan	Permissible Tangential Displacement				0.5	mm
303	WOBrad	Permissible Excentricity of Code Disc	MPC = 0x4 MPC = 0x5, 0x6			0.06 0.1	mm mm
<b>Bias Current Source, Reference Voltage, Power On Reset, Clock Oscillator</b>							
401	Vbg	Bandgap Voltage	TEST = 0x1F	1.18	1.25	1.32	V
402	Vref	Reference Voltage	TEST = 0x1F	45	50	55	%VPA
403	IBM	Reference Current	CIBM = 0x0 CIBM = 0xF IBM calibrated	-370 -220	-200	-100 -180	µA µA µA
404	VPDon	Turn-on Threshold VPD (power on release)	increasing voltage at V(VPD)	3.7	4	4.3	V
405	VPDoff	Turn-off Threshold VPD (power down reset)	decreasing voltage at V(VPD)	3	3.5	3.8	V
406	VPDhys	Hysteresis	VPDhys = VPDon - VPDoff	0.35			V
407	fosc	Clock Frequency	TEST=0x26, fosc = 64*f(HCLK), IBM aligned	22	26	30	MHz
<b>Signal Conditioning Master and Noniuspur (x = M, N)</b>							
501	GC	Adjustable Gain Range	GC_x = 0x0 GC_x = 0x1 GC_x = 0x2 GC_x = 0x3		4.4 7.7 12.4 20.6		
502	GF	Adjustable Fine Gain Range	GF_x = 0x00 GF_x = 0x20 GF_x = 0x3F		1 4.4 19		
503	GX	Adjustable Gain(SIN)/Gain(COS)	GX_x = 0x00 GX_x = 0x3F GX_x = 0x7F	9	0 10 -9	-8.5	% % %
504	VOS	Adjustable Offset Calibration	VOS_x = 0x3F VOS_x = 0x7F	65	70 -70	-65	mV mV
505	PHM	Adjustable Phase Calibration Master Track	PH_M = 0x3F PH_M = 0x7F	6	6.5 -6.5	-6	° °

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## ELECTRICAL CHARACTERISTICS

Operating conditions: VPD, VPA = 5 V ±10%, Tj = -40... 125°C, IBP calibrated to 200 µA, reference is VNA = VND, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
506	PHN	Adjustable Phase Calibration Nonius Track	PH_N = 0x3F PH_N = 0x7F	12	12.5 -12.5	-12	° °
507	Vampl	Signal Level Controller	chip internally, Vampl = Vpp(PSINx)+Vpp(NSINx), ENAC = 1	3.2	4	4.8	Vss
508	Vae()lo	Signal Monitoring Threshold lo	Vae()lo = Vpp(PSINx)+Vpp(NSINx)	1.2		2.8	Vpp
509	Vae()hi	Signal Monitoring Threshold hi	Vae()hi = Vpp(PSINx)+VPP(NSINx)	5		6.3	Vpp
<b>Sine-To-Digital Conversion</b>							
601	Aabs	Absolute Angular Accuracy	ideal input signals, reference to 12 Bit of sine period			2	LSB
602	Arel	Relative Angular Accuracy	FILT = 0x2 FILT = 0x7 ideal input signals, reference to 12 Bit of sine period, f = 1 KHz			2 1/4	LSB LSB
<b>Nonius Calculation</b>							
701	Pnon	Permissible Track deviation Master vers. Nonius	16 periods, MPC = 0x4 32 periods, MPC = 0x5 64 periods, MPC = 0x6 referenced to 360° of Master sine period			10 5 2.5	DEG DEG DEG
<b>Digital Output Port PA1..3, MTC, SCL, SDA</b>							
801	Vs()hi	Saturation Voltage hi Pins PA1..3, MTC	Vs()hi = V(VPD) - V(), I() = -4 mA			0.4	V
802	Vs()lo	Saturation Voltage lo	I() = 4 mA versus VND			0.4	V
803	Isc()hi	Short-Circuit Current hi Pins PA1..3, MTC	V() = V(VND), 25 °C	-90	-50		mA
804	Isc()lo	Short-Circuit Current lo	V() = V(VPD), 25 °C		50	90	mA
805	tr()	Rise Time	CL = 50 pF			60	ns
806	tf()	Fall Time	CL = 50 pF			60	ns
807	Ilk(PA3)	Leakage Current at PA3	MODEA=0, PA0 = hi	-5		5	µA
808	f(SCL)	Frequency at SCL	normal mode during start-up		80 60		kHz kHz
<b>Digital Input Port PA0..2, MTD, SCL, SDA</b>							
901	Vt()hi	Threshold Voltage hi				2	V
902	Vt()lo	Threshold Voltage lo		0.8			V
903	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo	150			mV
904	Ipu()	Pull-Up Current Pins PA0..2, MTD	V() = 0 V ... V(VPD)-1 V	-60	-30	-6	µA
905	Ipu()	Pull-Up Current Pins SCL, SDA	V() = 0 V ... V(VPD)-1 V	-750	-300	-75	µA
906	f()	Permissible Input Frequency				10	MHz
<b>Analog/Digital Output Port PB0..3</b>							
A01	I()buf	Analog Driver Current		-1		1	mA
A02	fg()ana	Analog Bandwidth			100		kHz
A03	Isc()hi,ana	Analog Short-Circuit Current hi	V() = V(VND)			-1.5	mA
A04	Isc()lo,ana	Analog Short-Circuit Current lo	V() = V(VPD)	1.5			mA
A05	Rout(),ana	Output Resistor, Analog Mode	I() = 1 mA			500	Ω
A06	Vs()hi,dig	Digital Saturation Voltage hi	Vs() = V(VPD) - V(), I() = -4 mA			0.5	V
A07	Vs()lo,dig	Digital Saturation Voltage lo	I() = 4 mA			0.5	V
A08	Isc()hi,dig	Short-Circuit Current hi	V() = V(VPD)	-60	-35		mA
A09	Isc()lo,dig	Short-Circuit Current lo	V() = V(VND)		45	70	mA
A10	tr()	Rise Time	CL = 50 pF			50	ns
A11	tf()	Fall Time	CL = 50 pF			50	ns
A12	Ipu(PB3)	Pull-Up Current	V() = 0 V...V(VPD) - 1 V, MODEB = 0x0..0x3	-60	-30	-6	µA
A13	Ilk()	Leakage Current	MODEB = 0x7	-5		5	µA



## OPERATING CONDITIONS: Multiturn Interface

Item No.	Symbol	Parameter	Conditions	Min.   Max.		Unit
				Min.	Max.	
<b>Multiturn Interface (Figure 1)</b>						
I001	$t_{MTC}$	Clock Period		6.4		us
I002	$t_{sMD}$	Setup Time: Data valid before MTC hi→lo		50		ns
I003	$t_{hMD}$	Hold Time: Data stable after MTC hi→lo		50		ns
I004	$t_{tos}$	Timeout		20		us
I005	$t_{cycle}$	Cycle Time	CHK_MT=1	1	5	ms

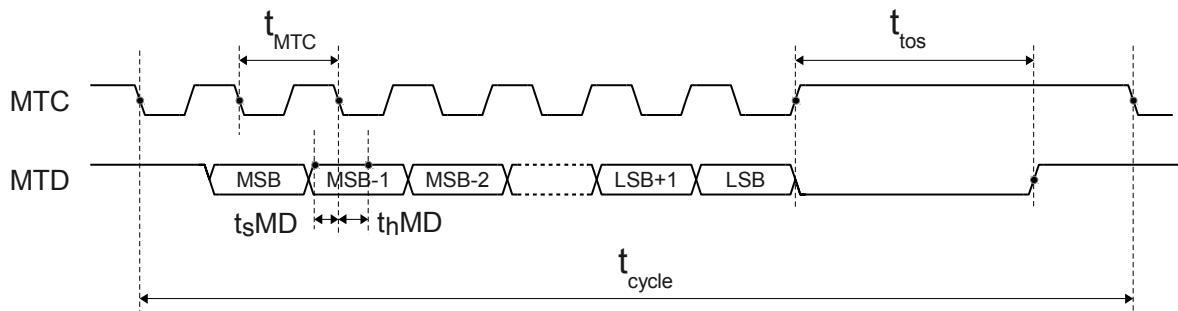


Figure 1: Timing multiturn interface, MODE\_MT/=0

## OPERATING CONDITIONS: I/O Interface

Item No.	Symbol	Parameter	Conditions	Min.   Max.		Unit
				Min.	Max.	
<b>SPI-Interface (Figure 2)</b>						
I101	$T_{SCK}$	Permissible Clock Period	see Elec. Char. No.: 906	1/f()		ns
I102	$t_{NCS}$	Setup Time: NCS lo before SCK hi $\rightarrow$ lo		50		ns
I103	$tp1$	Propagation Delay: MISO hi after NCS lo $\rightarrow$ hi		30		ns
I104	$t_{IS}$	Setup Time: MOSI stable before SCK lo $\rightarrow$ hi		30		ns
I105	$t_{SI}$	Hold Time: MOSI stable after SCK lo $\rightarrow$ hi		30		ns
I106	$tp2$	Propagation Delay: MISO stable after SCK hi $\rightarrow$ lo		30		ns
I107	$t_{CC}$	Wait Time: between NCS lo $\rightarrow$ hi and NCS hi $\rightarrow$ lo		500		ns
<b>BiSS-Interface (Figure 3)</b>						
I108	$t_{tos}$	Timeout		80	20000	ns
I109	$t_{MAS}$	Permissible Clock Period		100	$2 \times t_{tos}$	ns
I110	$t_{MASH}$	Clock Signal Hi Level Duration		50	$t_{tos}$	ns
I111	$t_{MASI}$	Clock Signal Lo Level Duration		50		ns
<b>SSI-Interface (Figure 4)</b>						
I112	$t_{tos}$	Timeout		20000		ns
I113	$t_{MAS}$	Permissible Clock Period		250	$2 \times t_{tos}$	ns
I114	$t_{MASH}$	Clock Signal Hi Level Duration		125	$t_{tos}$	ns
I115	$t_{MASI}$	Clock Signal Lo Level Duration		125		ns

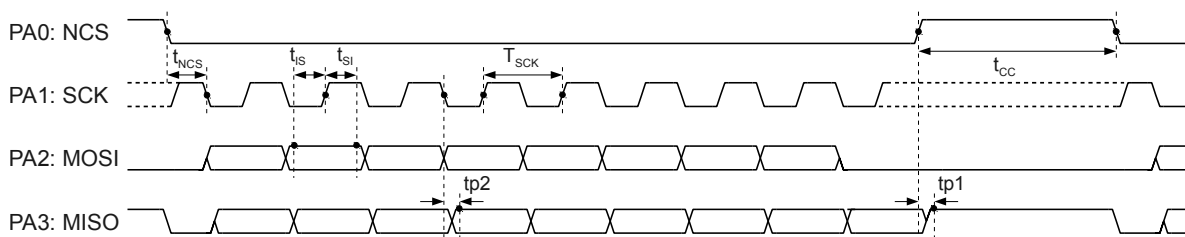


Figure 2: Timing SPI interface

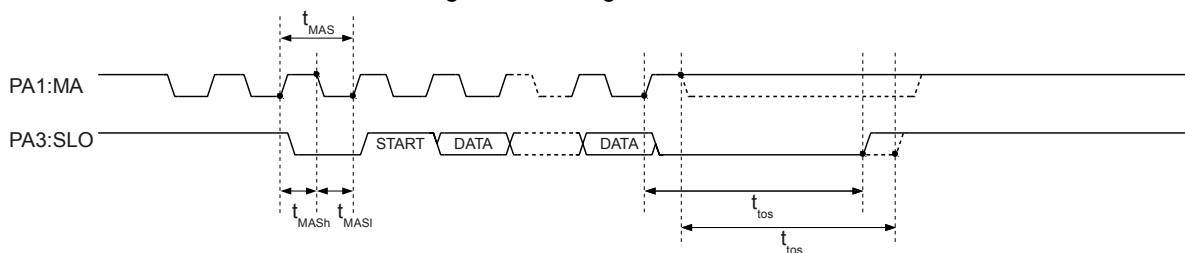


Figure 3: Timing BiSS interface

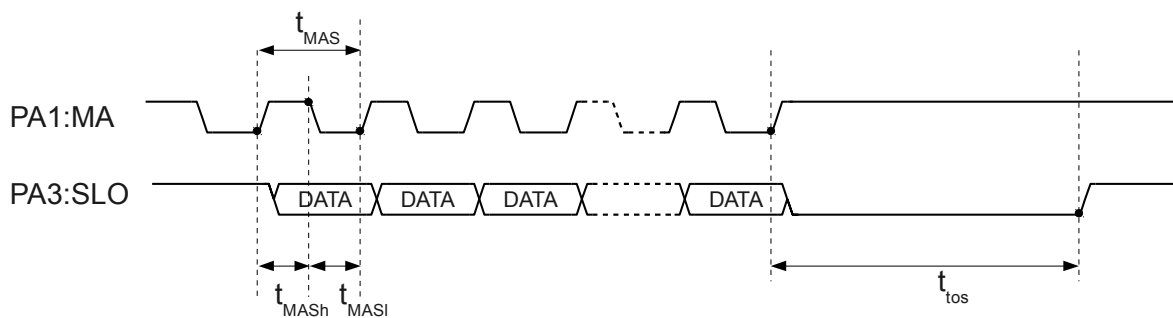


Figure 4: Timing SSI interface

## PRINCIPLE OF MEASUREMENT

An absolute position measuring system consists of a magnetized code carrier and an iC-MU which integrates Hall sensors for signal scanning, signal conditioning, and interpolation in one single device. iC-MU can be used in rotative and linear measurement systems.

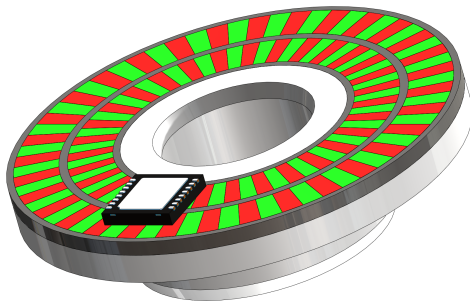


Figure 5: Rotative position measurement system



Figure 6: Linear position measurement system

### Rotative measuring system

The magnetic code carrier consists of two magnetic encoder tracks. The outer track comprises an even number of alternately magnetized poles and is used for high-precision position definition. This is thus called the master track. The second inside track has one pole pair less than the outer track and is thus referred to as the nonius track. This track is used to calculate an absolute position within one revolution of the pole disc. To this end, the difference in angle between the two tracks is calculated.

Number of pole pairs		16	32	64
Master track diameter	[mm]	13,04	26,08	52,15
Chip center to axis center	[mm]	4,72	11,24	24,28
Nonius track diameter	[mm]	5,84	18,88	44,95
Master track pole width	[mm]	1,28	1,28	1,28
Nonius track pole width	[mm]	0,61	0,96	1,12

Table 6: Pole disc dimensions in mm for rotative systems

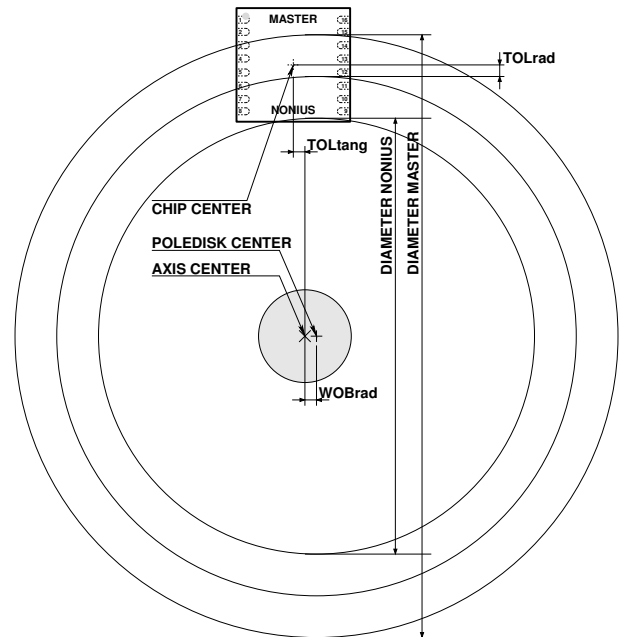


Figure 7: Definition of system measurements

The Hall sensors of iC-MU span one pole pair of the code carrier. The pole width of the master track is defined by the distance of the Hall sensors and is 1.28 mm. The position of the sensors on the upper chip edge has been optimized for 32 pole pairs. Accordingly, the Hall sensors generate a periodic sine and cosine signal with a cycle length of 2.56 mm. The scan diameter can be computed from the number of pole pairs. The diameter of the pole disc although depends on other mechanical requirements and should be approx. 3 mm greater than the scan diameter. A specific diameter for the master and nonius tracks is derived depending on the number of configured pole pairs.

The distance between the hall sensors of the nonius track and the master track is stipulated as being 3.6 mm by the evaluation device. The scan diameters of the nonius track can be seen in Table 6.

### Linear measuring system

With a linear nonius system the pole width of the master track is also 1.28 mm. The pole width of the nonius track is defined by the number of pole pairs with

$$p_{\text{nonius}} = 1.28 \text{ mm} * \frac{\text{number of poles}_{\text{master}}}{\text{number of poles}_{\text{nonius}}}$$

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Number of pole pairs	16	32	64
Master track pole width [mm]	1,28	1,28	1,28
Nonius track pole width [mm]	1,365	1,321	1,300

Table 7: Linear scales, pole widths in mm

## CONFIGURATION PARAMETERS

### Analog parameters (valid for all channels)

CIBM: Bias current settings (p. 19)  
ENAC: Amplitude control unit activation (p. 20)

### Signal conditioning

GC\_M: Master gain range selection (p. 19)  
GF\_M: Master gain (p. 19)  
GX\_M: Master cosine signal gain adjustment (p. 19)  
VOSS\_M: Master sine offset adjustment (p. 20)  
VOSC\_M: Master cosine offset adjustment (p. 20)  
PH\_M: Master phase adjustment (p. 20)  
GC\_N: Nonius gain range selection (p. 19)  
GF\_N: Nonius gain (p. 19)  
GX\_N: Nonius cosine signal gain adjustment (p. 19)  
VOSS\_N: Nonius sine offset adjustment (p. 20)  
VOSC\_N: Nonius cosine offset adjustment (p. 20)  
PH\_N: Nonius phase adjustment (p. 20)

### Digital parameters

TEST: Adjustment modes/iC-Haus test modes (p. 21)  
CRC16: EEPROM configuration data checksum (p. 22)  
CRC8: EEPROM offset and preset data checksum (p. 22)  
NCHK\_CRC: Cyclic check of CRC16 and CRC8 (p. 22)  
BANKSEL: Serial Access: Bankregister (p. 45)  
RPL: Register Access Control (p. 49)  
RPL\_RESET: Serial Access: Register for reset register access restriction (p. 49)  
EVENT\_COUNT: Serial Access: Eventcounter (p. 53)  
HARD\_REV: serial address: revision code (p. 48)

### Configurable I/O interface

MODEA: I/O port A configuration (p. 25)  
MODEB: I/O port B configuration (p. 25)  
PA0\_CONF: Configurable commands to pin PA0 A (p. 54)  
ROT: Direction of rotation (p. 44)  
OUT\_MSB: Output shift register configuration: MSB used bits (p. 27)  
OUT\_LSB: Output shift register configuration: LSB used bits (p. 27)  
OUT\_ZERO: Output shift register configuration: number of zeros inserted after the used bits and before an error/warning (p. 27)  
MODE\_ST: Data output (p. 26)  
GSSI: Gray/binary data format (p. 30)  
RSSI: Ring operation (p. 30)

### Multiturn interface

MODE\_MT: Multiturn mode (p. 38)  
SBL\_MT: Multiturn synchronization bit length (p. 38)  
CHK\_MT: Cyclic check of the multiturn value (p. 39)  
GET\_MT: Access Multiturn-Sensor via MT-Sensor via I/O-Interface (S. 41)  
ROT\_MT: Direction of rotation external multiturn (p. 39)  
ESSI\_MT: Error Bit external multiturn (p. 39)  
SPO\_MT: Offset external multiturn (p. 39)

### Converter and nonius calculation

FILT: Digital filter settings (p. 35)  
MPC: Master period count (p. 35)  
LIN: Linear scanning (p. 36)  
SPO\_x: Offset of nonius to master ( $x=BASE,0-14$ ) (p. 36)  
NCHK\_NON: Cyclic check of the nonius value (low active) (p. 37)

### Incremental output ABZ, STEP/DIR and CW/CCW

RESABZ: Incremental interface resolution ABZ,STEP-DIR,CW/CCW (p. 42)  
LENZ: Index pulse length (p. 43)  
INV\_A: A/STEP/CW signal inversion (p. 42)  
INV\_B: B/DIR/CCW signal inversion (p. 42)  
INV\_Z: Z/NCLR signal inversion (p. 42)  
SS\_AB: System AB step size (p. 43)  
FRQAB: AB output frequency (p. 43)  
CHYS\_AB: Converter hysteresis (p. 43)  
ENIF\_AUTO: Incremental interface enable (p. 43)

### UVW commutation signals

PPUVW: Number of commutation signal pole pairs (p. 44)  
PP60UVW: Commutation signal phase position (p. 44)  
OFF\_UVW: Commutation signal start angle (p. 44)  
OFF\_COM: serial address: absolute position offset for UVW calculation engine changed by nonius (S. 44)

### Status/command registers and error monitoring

CMD\_MU: serial address: command register (p. 52)  
STATUS0: serial address: status register 0 (p. 50)  
STATUS1: serial address: status register 1 (p. 50)  
CFGEW: Error and warning bit configuration (p. 50)  
EMTD: Minimum error message duration (p. 51)  
ACC\_STAT: Outputconfiguration status register (S. 50)  
ACRM\_RES: Automatic reset with master track amplitude errors (p. 37)

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## BiSS-ID/Profile-ID

REVISION: BiSS revision ID (p. 18)  
MANUFACTURER: BiSS manufacturer ID (p. 18)  
EDSBANK: BiSS-EDSBANK (p. 18)  
PROFILE\_ID: BiSS profile ID (p. 18)  
SERIAL: BiSS serial number (p. 18)

## Preset function

OFF\_ABZ: Offset Absolute position offset for ABZ calculation engine (p. 56)  
OFF\_POS: serial address: absolute position offset for ABZ calculation engine changed by nonius/multiturn (p. 56)  
PRES\_POS: Preset position for ABZ section (p. 56)

## REGISTER ASSIGNMENTS (EEPROM)

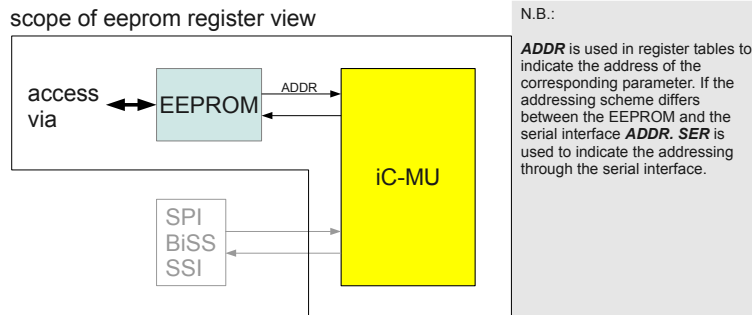


Figure 8: Scope of register mapping EEPROM

### Register assignment (EEPROM)

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Signal Conditioning</b>								
0x00	GC_M(1:0)		GF_M(5:0)					
0x01	GX_M(6:0)							
0x02	VOSS_M(6:0)							
0x03	VOSC_M(6:0)							
0x04	PH_M(6:0)							
0x05	ENAC	CIBM(3:0)						
0x06	GC_N(1:0)		GF_N(5:0)					
0x07	GX_N(6:0)							
0x08	VOSS_N(6:0)							
0x09	VOSC_N(6:0)							
0x0A	PH_N(6:0)							
<b>Digital Parameters</b>								
0x0B	MODEB(2:0)			MODEA(2:0)				
0x0C	CFGEW(7:0)							
0x0D	ACC_STAT	NCHK_CRC	NCHK_NON	ACRM_RES	EMTD(2:0)			
0x0E	ESSI_MT(1:0)		ROT_MT	LIN	FILT(2:0)			
0x0F	SPO_MT(3:0)				MPC(3:0)			
0x10	GET_MT	CHK_MT	SBL_MT(1:0)		MODE_MT(3:0)			
0x11	OUT_ZERO(2:0)			OUT_MSB(4:0)				
0x12	GSSI	RSSI	MODE_ST(1:0)		OUT_LSB(3:0)			
0x13	RESABZ(7:0)							
0x14	RESABZ(15:8)							
0x15	ROT	SS_AB(1:0)		ENIF_AUTO	FRQAB(2:0)			
0x16	LENZ(1:0)		CHYS_AB(1:0)	PP60UVW	INV_A	INV_B	INV_Z	
0x17	RPL(1:0)		PPUVW(5:0)					
<b>TEST</b>								
0x18	TEST(7:0)							
<b>TRACK-OFFSET</b>								
0x19	SPO_0(3:0)			SPO_BASE(3:0)				
0x1A	SPO_2(3:0)			SPO_1(3:0)				



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OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1B		SPO_4(3:0)				SPO_3(3:0)		
0x1C		SPO_6(3:0)				SPO_5(3:0)		
0x1D		SPO_8(3:0)				SPO_7(3:0)		
0x1E		SPO_10(3:0)				SPO_9(3:0)		
0x1F		SPO_12(3:0)				SPO_11(3:0)		
0x20		SPO_14(3:0)				SPO_13(3:0)		
CRC16								
0x21		CRC16(15:8)						
0x22		CRC16(7:0)						
OFFSET/PRESET								
0x23		OFF_ABZ(3:0)						
0x24		OFF_ABZ(11:4)						
0x25		OFF_ABZ(19:12)						
0x26		OFF_ABZ(27:20)						
0x27		OFF_ABZ(35:28)						
0x28		OFF_UVW(3:0)						
0x29		OFF_UVW(11:4)						
0x2A		PRES_POS(3:0)						
0x2B		PRES_POS(11:4)						
0x2C		PRES_POS(19:12)						
0x2D		PRES_POS(27:20)						
0x2E		PRES_POS(35:28)						
CRC8								
0x2F		CRC8(7:0)						
PA0_CONF								
0x30		PA0_CONF(7:0)						
BiSS Profile and Serial number								
0x31		EDSBANK(7:0) = 0x01						
0x32		PROFILE_ID(7:0)						
0x33		PROFILE_ID(15:8)						
0x34		SERIAL(7:0)						
0x35		SERIAL(15:8)						
0x36		SERIAL(23:16)						
0x37		SERIAL(31:24)						
Device Identification								
0x38		REVISION(7:0)						
0x39		REVISION(15:8)						
0x3A		REVISION(23:16)						
0x3B		REVISION(31:24)						
0x3C		REVISION(39:32)						
0x3D		REVISION(47:40)						
0x3E		MANUFACTURER(7:0)						
0x3F		MANUFACTURER(15:8)						
Notes:	Register assignment for serial access through SPI/BiSS s.p. 45							

Table 8: Register assignment (EEPROM)

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## Special BiSS registers

For further information on parameters, see BiSS Interface Protocol Description (C Mode) [www.ichaus.de/product/iC-MU](http://www.ichaus.de/product/iC-MU).

<b>REVISION(7:0)</b>	Addr. 0x38; bit 7:0
<b>REVISION(15:8)</b>	Addr. 0x39; bit 7:0
<b>REVISION(23:16)</b>	Addr. 0x3A; bit 7:0
<b>REVISION(31:24)</b>	Addr. 0x3B; bit 7:0
<b>REVISION(39:32)</b>	Addr. 0x3C; bit 7:0
<b>REVISION(47:40)</b>	Addr. 0x3D; bit 7:0
<b>REVISION(7:0)</b>	Addr. SER:0x78; bit 7:0
<b>REVISION(15:8)</b>	Addr. SER:0x79; bit 7:0
<b>REVISION(23:16)</b>	Addr. SER:0x7A; bit 7:0
<b>REVISION(31:24)</b>	Addr. SER:0x7B; bit 7:0
<b>REVISION(39:32)</b>	Addr. SER:0x7C; bit 7:0
<b>REVISION(47:40)</b>	Addr. SER:0x7D; bit 7:0
Code	Description
0x000000000000	Device ID
...	
0xFFFFFFFFFFFF	

Table 9: REVISION: Device ID

<b>MANUFACTURER(7:0)</b>	Addr. 0x3E; bit 7:0
<b>MANUFACTURER(15:8)</b>	Addr. 0x3F; bit 7:0
<b>MANUFACTURER(7:0)</b>	Addr. SER:0x7E; bit 7:0
<b>MANUFACTURER(15:8)</b>	Addr. SER:0x7F; bit 7:0
Code	Description
0x0000	Manufacturer ID
...	
0xFFFF	

Table 10: MANUFACTURER: Manufacturer ID

<b>EDSBANK(7:0)</b>	Addr. 0x31; bit 7:0
<b>EDSBANK(7:0)</b>	Addr. SER:0x41; bit 7:0
Code	Description
0x00	EDSBANK: has to be set to 0x01 for iC-MU
...	
0xFF	

Table 11: EDSBANK: Start of EDS-part

<b>PROFILE_ID(7:0)</b>	Addr. 0x32; bit 7:0
<b>PROFILE_ID(15:8)</b>	Addr. 0x33; bit 7:0
<b>PROFILE_ID(7:0)</b>	Addr. SER:0x42; bit 7:0
<b>PROFILE_ID(15:8)</b>	Addr. SER:0x43; bit 7:0
Code	Description
0x0000	Profile ID
...	
0xFFFF	

Table 12: PROFILE\_ID: Profile ID

<b>SERIAL(7:0)</b>	Addr. 0x34; bit 7:0
<b>SERIAL(15:8)</b>	Addr. 0x35; bit 7:0
<b>SERIAL(23:16)</b>	Addr. 0x36; bit 7:0
<b>SERIAL(31:24)</b>	Addr. 0x37; bit 7:0
<b>SERIAL(7:0)</b>	Addr. SER:0x44; bit 7:0
<b>SERIAL(15:8)</b>	Addr. SER:0x45; bit 7:0
<b>SERIAL(23:16)</b>	Addr. SER:0x46; bit 7:0
<b>SERIAL(31:24)</b>	Addr. SER:0x47; bit 7:0
Code	Description
0x00000000	Serial number
...	
0xFFFFFFFF	

Table 13: SERIAL: Serial number

## SIGNAL CONDITIONING FOR MASTER AND NONIUS CHANNELS: x = M,N

### Bias current source

The calibration of the bias current source in test mode  $TEST=0x1F$  is prerequisite for adherence to the given electrical characteristics and also instrumental in the determination of the chip timing (e.g. SCL clock frequency). For the calibration the current out of pin PB2 into VNA must be measured, and register bits CIBM changed until the current is calibrated to 200  $\mu A$ .

CIBM(3:0) Addr. 0x05; bit 3:0	
Code	Description
0x0	-40 %
...	...
0x8	0 %
0x9	+5 %
...	...
0xF	+35 %

Table 14: Calibrating the bias current

### Gain settings

iC-MU has signal conditioning features that can compensate for signal and adjustment errors. The Hall signals are amplified in two stages. The gain of both amplification stages is automatically controlled when the bit ENAC is set to '1'. The register bits GC\_x and GF\_x have no effect. In the case of a deactivated automatic gain control (ENAC='0') the gain must be set manually. First, the approximate field strength range must be selected in which the Hall sensor is to be operated. The first amplifier stage can be programmed in the following ranges:

GC_M(1:0) Addr. 0x00; bit 7:6	
GC_N(1:0) Addr. 0x06; bit 7:6	
Code	Coarse gain
0x0	4.4
0x1	7.8
0x2	12.4
0x3	20.7

Table 15: Selection of the Hall signal amplification range

The second amplifier stage can be varied within a wide range.

GF_M(5:0) Addr. 0x00; bit 5:0	
GF_N(5:0) Addr. 0x06; bit 5:0	
Code	Fine gain
0x00	1,000
0x01	1,048
...	$\exp(\frac{\ln(20)}{64} \cdot GF_x)$
0x3F	19,08

Table 16: Hall signal amplification

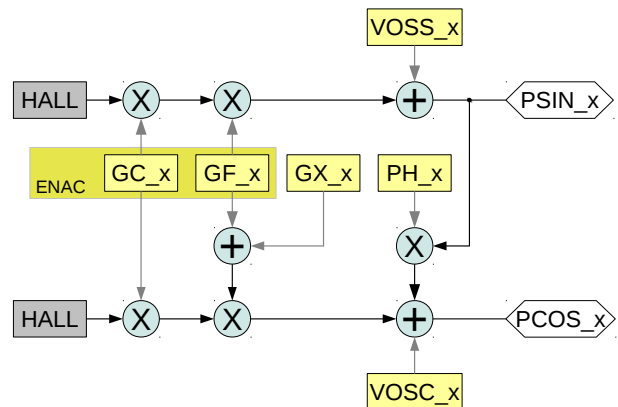


Figure 9: Conditioning of hall voltages

Register GX\_x enables the sensitivity of the sine channel in relation to the cosine channel to be corrected. The amplitude of the cosine channel is adapted to the amplitude of the sine channel. The cosine amplitude can be corrected within a range of approx.  $\pm 10\%$ .

GX_M(6:0) Addr. 0x01; bit 6:0	
GX_N(6:0) Addr. 0x07; bit 6:0	
Code	Description
0x00	1,000
0x01	1,0015
...	$\exp(\frac{\ln(20)}{2048} \cdot GX_x)$
0x3F	1,0965
0x40	0,9106
...	$\exp(-\frac{\ln(20)}{2048} \cdot (128 - GX_x))$
0x7F	0,9985

Table 17: Cosine gain adjustment

The integrated amplitude control unit can be activated using bit ENAC. In this case the differential signal amplitude is regulated to 2 Vpp; the values of GF\_x have no effect here.

ENAC		Addr. 0x05; bit 7
Code	Description	
0	Amplitude control not active ( <i>constant</i> )	
1	Amplitude control active ( $\sin^2 + \cos^2$ )	

Table 18: Amplitude control unit activation

After startup the gain is increased until the set amplitude is obtained. If the input amplitude is altered by the distance between the magnet and sensor being varied, or if there is a change in the supply voltage or temperature, the gain is automatically adjusted. The conversion of the sine signals into high-resolution quadrature signals thus always takes place at optimum amplitude.

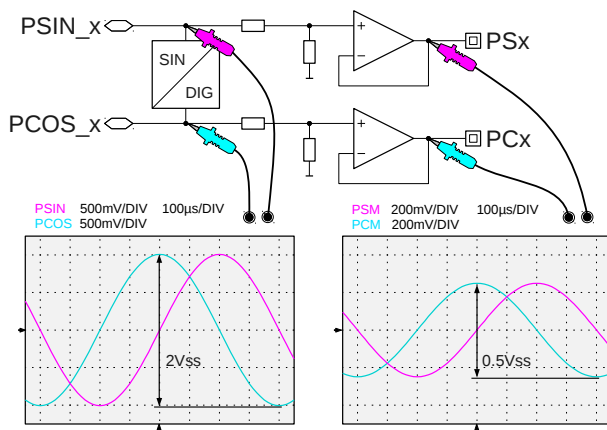


Figure 10: Definition of differential amplitude

### Offset compensation

If there is an offset in the sine or cosine signal, possibly caused by a magnet not being precisely adjusted, for instance, this can be corrected by registers VOSS\_x and VOSC\_x. The output voltage can be shifted in each case by  $\pm 63$  mV in order to compensate for the offset.

VOSS_M(6:0)		Addr. 0x02; bit 6:0
VOSS_N(6:0)		Addr. 0x08; bit 6:0
VOSC_M(6:0)		Addr. 0x03; bit 6:0
VOSC_N(6:0)		Addr. 0x09; bit 6:0
Code	Description	
0x00	0 mV	
0x01	1 mV	
...	...	
0x3F	63 mV	
0x40	0 mV	
0x41	-1 mV	
...	...	
0x7F	-63 mV	

Table 19: Sine and cosine offset adjustment

### Phase adjustment

The phase between sine and cosine is adjusted by PH\_x (6:0). The compensation range for the master track is approx.  $\pm 6^\circ$ . The compensation range for the nonius track is nearly twice as large and is approx.  $\pm 11.25^\circ$ .

PH_M(6:0)		Addr. 0x04; bit 6:0
Code	Function	
0x00	0°	
...	+ 6°*PH_M/63	
0x3F	+ 6°	
0x40	0°	
...	- 6°*(PH_M-64)/63	
0x7F	- 6°	

Table 20: Master track phase adjustment

PH_N(6:0)		Addr. 0x0A; bit 6:0
Code	Function	
0x00	0°	
...	+ 11,25°*PH_N/63	
0x3F	+ 11,25°	
0x40	0°	
...	- 11,25°*(PH_N-64)/63	
0x7F	- 11,25°	

Table 21: Nonius track phase adjustment

## ANALOG SIGNAL CONDITIONING FLOW: x = M,N

For the purpose of signal conditioning iC-MU has several settings that make internal reference values and the amplified Hall voltages of the individual sensors accessible at the outer pins of PORT B for measurement. This allows the settings of the amplifier (GC\_x, GF\_x), the amplitude ratio of cosine to sine signal (GX\_x), and the offset (VOSS\_x, VOSC\_x) and phase (PH\_x) of the master (x = M) and nonius tracks (x = N) to be directly observed on the oscilloscope.

Test mode can be programmed using register TEST (address 0x18). The individual test modes are listed in Table 22 and 23.

### N.B.:

MODEB must be set to 0x0 before selecting a test mode.

Test Mode output signals					
Modus	TEST	Pin PB0	Pin PB1	Pin PB2	Pin MTC
Normal	0x00				
Analog REF	0x1F	VREF	VBG	IBM	-
Digital CLK	0x26	-	-	-	CLK

Table 22: Test modes for signal conditioning

### 1. Conditioning the BIAS current

First of all, the internal bias is set. The BIAS current is adjustable in the range of -40 % to +35% to compensate variations of this current and thus differences in characteristics between different iC-MU (e.g. due to manufacturing variations). The nominal value of 200 µA is measured as a short-circuit current at pin PB2 referenced to VNA in test mode 0x1F.

Additionally various internal reference voltages are available for measuring in this test mode. VREF corresponds to half the supply voltage (typically 2.5 V) and is used as a reference voltage for the hall sensor signals. VBG is the internal bandgap reference (1.25 V)

Alternatively the frequency at Pin MTC can be adjusted to 380 kHz using register value CIBM in test mode 0x26, if an analog measuring of the current is not possible.

Test mode output signals					
Modus	TEST	Pin PB0	Pin PB1	Pin PB2	Pin PB3
Normal	0x00				
Analog Master	0x01	PSM	NSM	PCM	NCM
Analog CNV_M	0x03	PSIN_M	NSIN_M	PCOS_M	NCOS_M
Analog Nonius	0x11	PSN	NSN	PCN	NCN
Analog CNV_N	0x13	PSIN_N	NSIN_N	PCOS_N	NCOS_N

Table 23: Testmodes and available output signals

The output signals of the signal path are available as differential signals with a mean voltage of half the supply voltage and can be selected for output according to Table 23.

### 2. Positioning of the sensor

Next, the sensor should be adjusted in relation to the magnetic code carrier. The value of MPC (Table 48) has to be selected according to the magnetic code carrier. The register values for VOSS\_x, VOSC\_x, GX\_x and PH\_x are set to 0. The chip position will now be displaced radially to the magnetic code carrier until the phase shift between the sine and cosine is 90°.

Depending on the mounting of the system it may be necessary to displace iC-MU tangentially to the magnetic code carrier to adjust the amplitude between the sine and cosine signals.

A fine adjustment of the analog signals is made with the registers described in the chapter SIGNAL CONDITIONING FOR MASTER AND NONIUS CHANNELS page 19.

The adjustment should be made in the order:

1. phase
2. amplitude
3. offset

### 3.a Test modes analog master and analog nonius

In these test modes the amplified, conditioned signals are presented to port B. These signals can be charged with a maximum of 1 mA and should not exceed a differential voltage of 0.5 Vpp.

### 3.b Test mode CNV\_x

In this test mode the sensor signals are present at port B as they are internally for further processing on the interpolator. The achievable interpolation accuracy is determined by the quality of signals PSIN\_x/NSIN\_x and PCOS\_x/NCOS\_x and can be influenced in this test mode by adjustment of the gain, amplitude ratio, offset, and phase. The signals must be tapped at high impedance.

### 4. Trackoffset SPON

After the analog adjustment of the master and nonius track the absolute system must be electrically calibrated for maximum adjustment tolerance. See page 36 ff.

## I2C INTERFACE AND STARTUP BEHAVIOR

### I2C interface / CRC

The multimaster-I2C interface enables read and write access to a serial EEPROM which uses an addressing scheme equal to an 24C01 EEPROM (e.g. 24C02, 256 bytes, 5V type with a 3.3V function).

The configuration data in the EEPROM in address range 0x00 to 0x20 and 0x30 to 0x3F is checked with a 16 bit CRC (CRC16). The start value for the CRC16 calculation is 1.

<b>CRC16(7:0)</b>	Addr. 0x21; bit 7:0
<b>CRC16(15:8)</b>	Addr. 0x22; bit 7:0
<b>CRC16(15:0)</b>	Addr. SER: no access;
Code	Meaning
...	CRC formed with CRC polynomial 0x11021*)
Notes:	*) $x^{16} + x^{12} + x^5 + 1$ , start value 0x1 This is equivalent to CRC-CCITT/CRC-16

Table 24: EEPROM data checksum

The offset and preset position for iC-MU's preset sequence is not part of the configuration data area. The data is located in address range 0x23 to 0x2E of the EEPROM and is checked separately with a 8-bit CRC (CRC8). The start value for the CRC8 calculation is 1.

<b>CRC8(7:0)</b>	Addr. 0x2F; bit 7:0
<b>CRC8(7:0)</b>	Addr. SER: no access;
Code	Meaning
...	CRC formed with CRC polynomial 0x197*)
Notes:	*) $x^8 + x^7 + x^4 + x^2 + x^1 + 1$ , start value 0x1

Table 25: Offset/preset data checksum

iC-MU calculates CRC8 and CRC16 automatically when writing the configuration to the EEPROM. The serial interface does not allow to access the CRC8 and CRC16 values. CRC16 and CRC8 are checked on startup. A cyclic check during operation can be configured with NCHK\_CRC. With the command CRC\_VER (s. Tab. 97) a CRC check can be explicitly requested. An error is signaled by status bit CRC\_ERR.

<b>NCHK_CRC</b>	Addr. 0x0D; bit 6
Code	Meaning
0	cyclical CRC check of CRC16 and CRC8
1	no cyclical CRC check

Table 26: Zyclic CRC check

## Startup behavior

After switching on the power (power-on reset) iC-MU reads the configuration data out from the EEPROM. If an error occurs during the EEPROM data readout (a CRC error or communication fault with the EEPROM), the current read-in is aborted and restarted. Following a third faulty attempt the read-in process is terminated and the internal iC-MU configuration register initialized as in Tab. 27. The addresses are referenced to the register allocation for an register access through the serial interface s. p. 45.

**N.B.:** After the third faulty attempt to read-in the configuration data from the EEPROM the default value of MODEA is set to BiSS or SPI depending on the logic level at pin PA0 (PA0=0 → BiSS, PA0=1 → SPI).

The amplitude control is started after the read-in of the EEPROM. To determine the absolute position a nonius calculation is started. An external multturn is read-in if configured. If there is an error the multturn read-in is repeated until no multturn error occurs. The Statusbit MT\_ERR is set in this case, register communication is possible. The ABZ/UVW-converter is only started if there was no CRC\_ERR, EPR\_ERR, MT\_ERR or MT\_CTR error during startup. The startup behaviour is described in picture 11.

Default values			
Bank	Addr. (serial access)	value	Meaning
0	0x05	0x88	Amplitude control active (ENAC=1), CIBM = 0%
0	0x0B	0x02	PA0=0 → BiSS interface (MODEA=0x2), ABZ Incremental (MODEB=0x0)
0		0x00	PA0=1 → SPI interface (MODEA=0x0), ABZ Incremental (MODEB=0x0)
0	0x0E	0x06	FILTER activated
0	0x0F	0x05	32 pole pairs master track
0	0x10	0x00	no Multiturn, Noniuscheck active
0	0x11	0xA5	5 bit Noniusinformation, 5 Zeros added
0	0x12	0x00	output with max. resolution
0	0x13	0xFF	resolution 16384 edges
0	0x14	0x0F	
0	0x15	0x13	up to 12000 rpm (SS_AB=0x1), 266ns minimum edge distance
0	0x16	0x10	90° Index, 0.08° Hysteresis
0	0x17	0x02	1 pole pair Polpaar commutation
-	0x78	0x4D	≈ M
-	0x79	0x55	≈ U
-	0x7A	HARD_REV	s. Tab. 87
-	0x7E	0x69	≈ i
-	0x7F	0x43	≈ C
Notes:	all other registers are preset with 0 Register assignment for register access through serial interface s. S. 45		

Table 27: Default configuration without the EEPROM

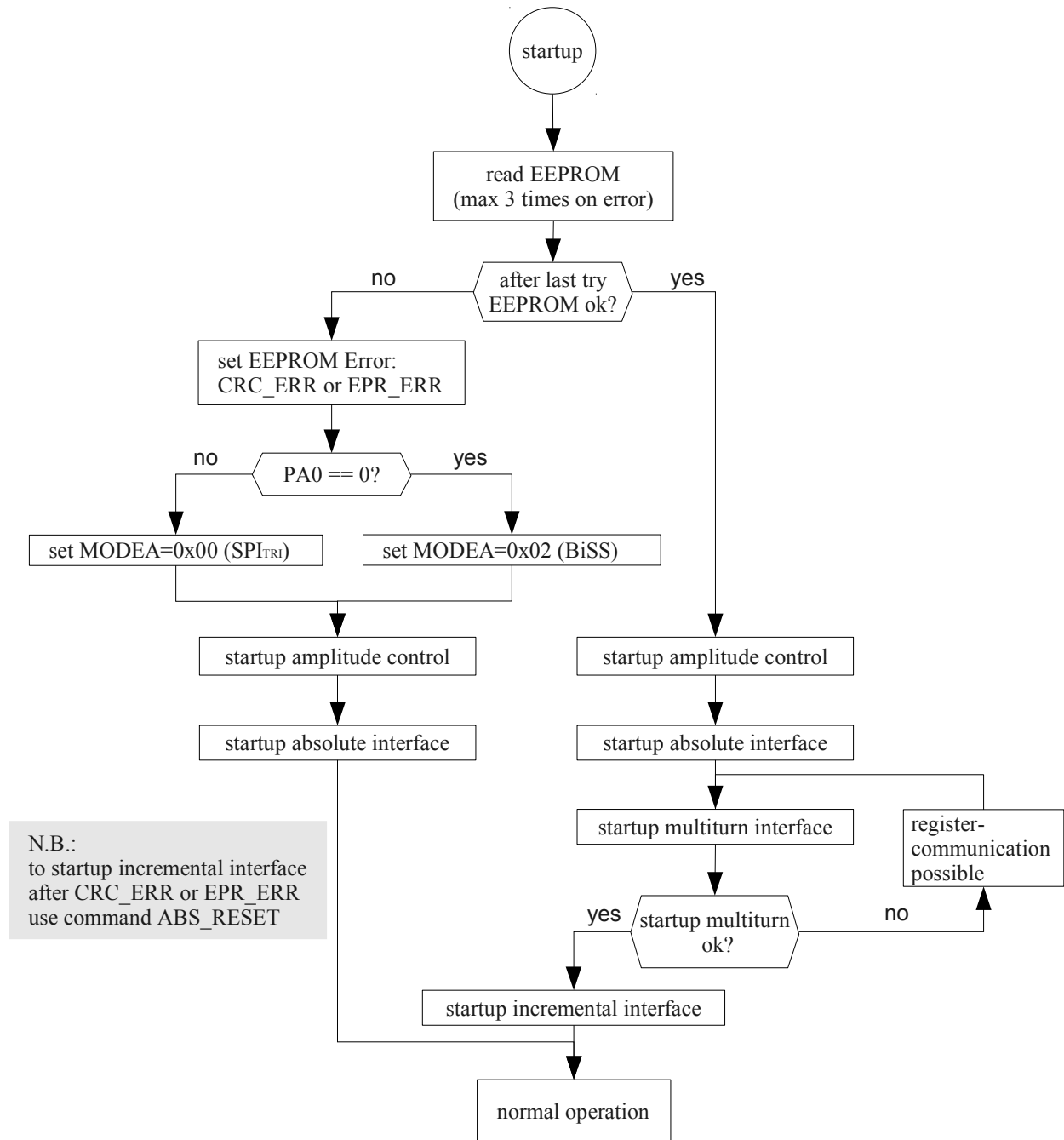


Figure 11: Startup behavior



## CONFIGURABLE I/O INTERFACE

### Setting the interfaces

iC-MU has several configurable output modes which can be set using parameters MODEA and MODEB. The pins at port A are set with MODEA. The choice of a serial interface at port A has also effect on the output of error and warning bits in the serial protocol see Table 31.

#### N.B.:

With an empty EEPROM or after the third faulty attempt to read-in the configuration data from the EEPROM the default value of MODEA is set to BiSS or SPI depending on the logic level at pin PA0 (PA0=0 → BiSS, PA0=1 → SPI).

MODEA(2:0) Addr. 0x0B; bit 2:0					
Code	PA0	PA1	PA2	PA3	Function
0x0	NCS	SCLK	MOSI	MISO	SPI <sub>TRI</sub>
0x1	NCS	SCLK	MOSI	MISO	SPI
0x2	NPRES	MA	SLI	SLO	BiSS
0x3	NPRES	A	B	Z	ABZ *)
0x4	NPRES	MA	SLI	SLO	SSI
0x5	NPRES	MA	SLI	SLO	SSI+ERRL
0x6	NPRES	MA	SLI	SLO	SSI+ERRH
0x7	NPRES	MA	SLI	SLO	ExtSSI

Note: \*) to save this configuration in the EEPROM see command SWITCH page 52 ff.

Table 28: Port A configuration

The pins at port B are set with MODEB.

MODEB(2:0) Addr. 0x0B; bit 6:4					
Code	PB0	PB1	PB2	PB3	Function
0x0	A	B	Z	NER	ABZ
0x1	U	V	W	NER	UVW
0x2	STEP	DIR	NCLR	NER	Step/Direction
0x3	CW	CCW	NCLR	NER	CW/CCW Incremental
0x4	NSN	PSN	PCN	NCN	SIN/COS Nonius
0x5	NSM	PSM	PCM	NCM	SIN/COS Master
0x6	-	-	-	-	reserved
0x7	-	-	-	-	tristate

Table 29: Port B configuration

#### N.B.:

It is not possible to select ABZ at port A and ABZ, Step/Direction or CW/CCW at port B simultaneously.

In operating modes ABZ, UVW, step/direction, and CW/CCW the position is output incrementally. In setting SIN/COS Master the master track analog signal is switched directly to the analog drivers. The signals of the nonius track are available on the drivers with setting SIN/COS Nonius.

## Serial interface

### Configuring the data format and data length

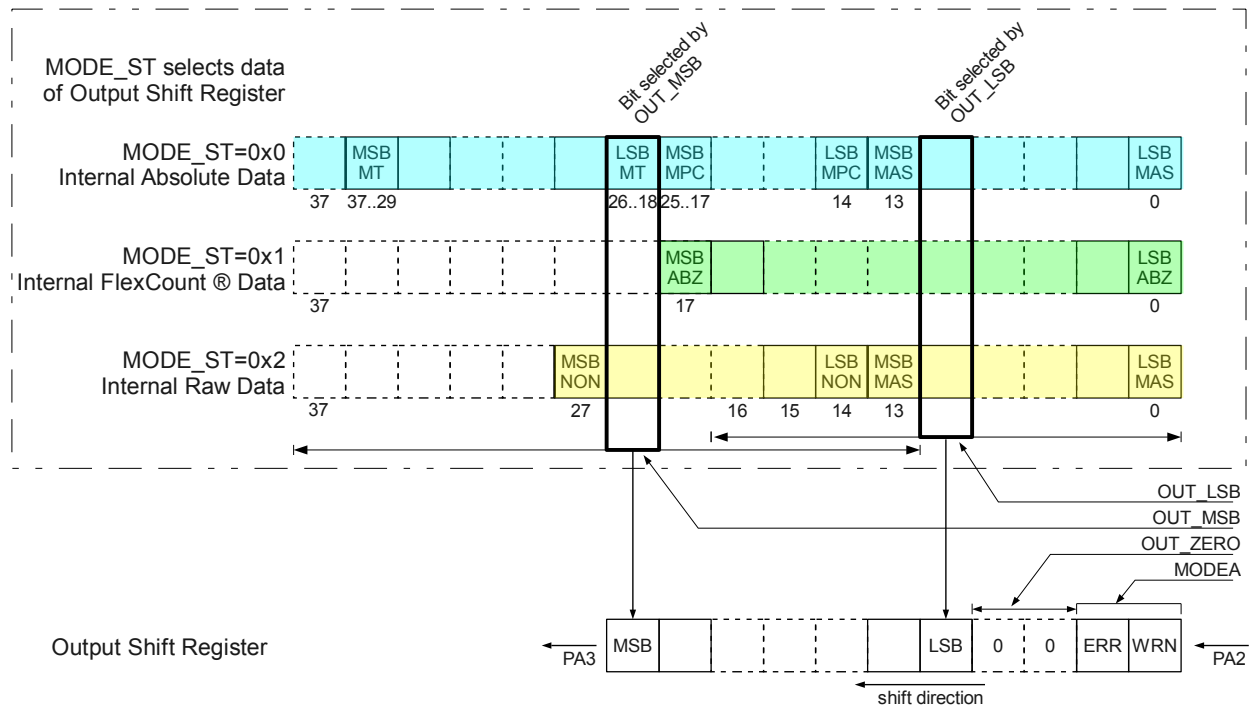


Figure 12: Determining the output data length

The structure of the output shift register is shown in Figure 12. The abbreviation MT stands for the multi-turn data, MPC is short for the number of master periods in bit, ABZ for the data whose resolution is specified by the parameter RESABZ (Table 67), NON for the data of the nonius track and MAS for the data of the master track. The numbering of the user data starts at the LSB with zero. OUT\_MSB and OUT\_LSB determine which part of the user data is output by the output shift register.

MODE\_ST selects the type of user data to be output through the output shift register.

MODE_ST(1:0) Addr. 0x12; bit 5:4	
Code	Description
0x0	output absolute position
0x1	output position in user resolution*) (Flexcount®)
0x2	output raw-data of Master- and Nonius track
0x3	reserved
Note:	*) resolution defined by RESABZ (Table 67)

Table 30: Selection of output data

The number of output bits is determined by parameters OUT\_MSB, OUT\_LSB, OUT\_ZERO and the error/warning bits (see Figure 12 and Table 31):

Data length = 13 + OUT\_MSB - OUT\_LSB + OUT\_ZERO + optional ERR/WRN (depending on MODEA)

There is an exception for the calculation of the output data length. If parameter MPC=12 and OUT\_LSB = 0, the number of output bits is given by:

data\_length\_2 = OUT\_MSB + OUT\_ZERO + ERR/WRN (depending on MODEA) - 2

MODEA(2:0) Addr. 0x0B; bit 2:0				
Function	Error		Warning	
	low active	high active	low active	high active
SPI	-	-	-	-
BiSS	x	-	x	-
SSI	-	-	-	-
SSI+ERRL	x	-	-	-
SSI+ERRH	-	x	-	-
ExtSSI	x	-	x	-

Table 31: MODEA: error/warning-bit within serial protocols

OUT\_MSB configures the bit of the user data which is output as MSB at pin PA3.

<b>OUT_MSB(4:0)</b> Addr. 0x11; bit 4:0	
Code	Description
0x00	MSB = Bit 13
0x01	MSB = Bit 14
...	...
0x18	MSB = Bit 37

Table 32: Selection of shift register MSB

OUT\_LSB determines the LSB of the user data being output through the output shift register.

<b>OUT_LSB(3:0)</b> Addr. 0x12; bit 3:0		
Code	Condition	Description
0x0	MPC = 12, OUT_MSB > 0x02 MPC ≠ 12	LSB = Bit 16 LSB = Bit 0
0x1	-	LSB = Bit 1
0x2	-	LSB = Bit 2
...	-	...
0xD	-	LSB = Bit 13
0xE	OUT_MSB > 0x00	LSB = Bit 14
0xF	OUT_MSB > 0x01	LSB = Bit 15

Table 33: Selection of shift register LSB

With OUT\_ZERO additional zeros to be inserted between the user data and the error/warning bit can be

configured. Parameter OUT\_ZERO can be used to achieve multiples of 8 bits when sensor data is output through the SPI interface.

<b>OUT_ZERO(2:0)</b> Addr. 0x11; bit 7:5	
Code	Description
0x0	no additional '0' Bit
0x1	1 additional '0' Bit
...	...
0x7	7 additional '0'-Bits

Table 34: Selection of additional ZEROs

The direction of rotation can be inverted with parameter ROT. The parameter affects the output of the data word through the serial interface in MODE\_ST=0x0 and 0x1, the ABZ-interface and the UVW-interface.

<b>ROT</b> Addr. 0x15; bit 7	
Code	Description
0	no inversion of direction of rotation
1	inversion of rotation
Note:	no effect in MODE_ST = 2 (raw-data) for the data output through the serial interface

Table 35: Inversion of the direction of rotation (for MT and ST data)

## BiSS C interface

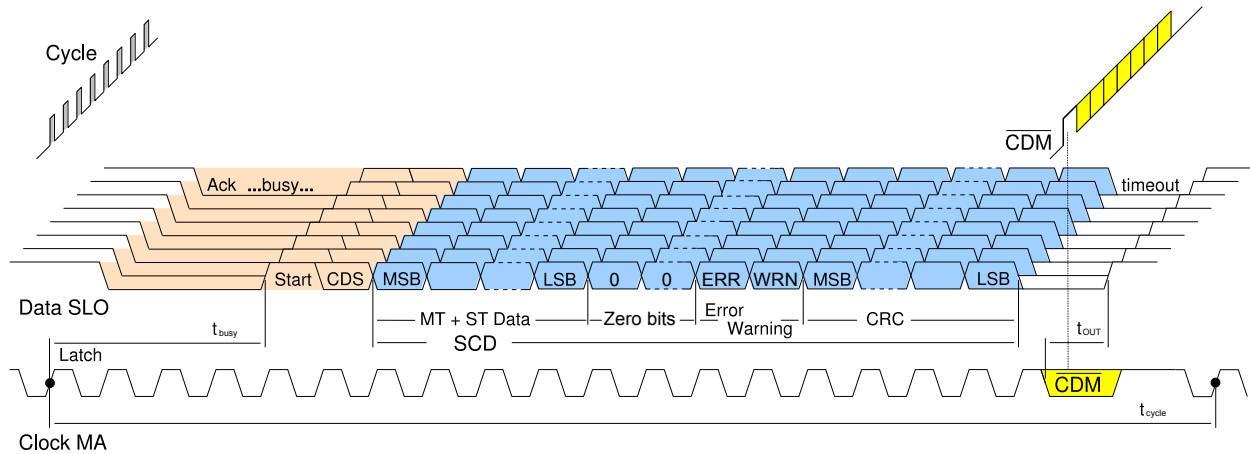


Figure 13: Example of BiSS line signals

MODEA	
Code	Description
0x2	BiSS-C

Table 36: MODEA: BiSS

In BiSS protocol iC-MU uses fixed CRC polynomials, see Table 37. The singlecycle data (SCD), i.e. the primary data which is newly generated and completely transmitted in each cycle, contains the position data (optional multiturn + singleturn) and the error and warning bit. The CRC value is output inverted.

The BiSS C interface has an adaptive sensor data timeout. Data is output in binary form. The error and warning bit is low active. Transmission of sensor and register data is implemented. iC-MU needs no processing time therefore  $t_{busy}$  is one master clock cycle. For further information regarding the BiSS-C-protocol visit [www.biss-interface.com](http://www.biss-interface.com).

data-channel*)	CRC HEX Code	Polynomial
SCD (sensor)	0x43	$x^6+x^1+x^0$
CDM, CDS (register)	0x13	$x^4+x^1+x^0$
Note:	*) explanation s. BiSS-C specification	

Table 37: BiSS CRC polynomials

## SSI interface

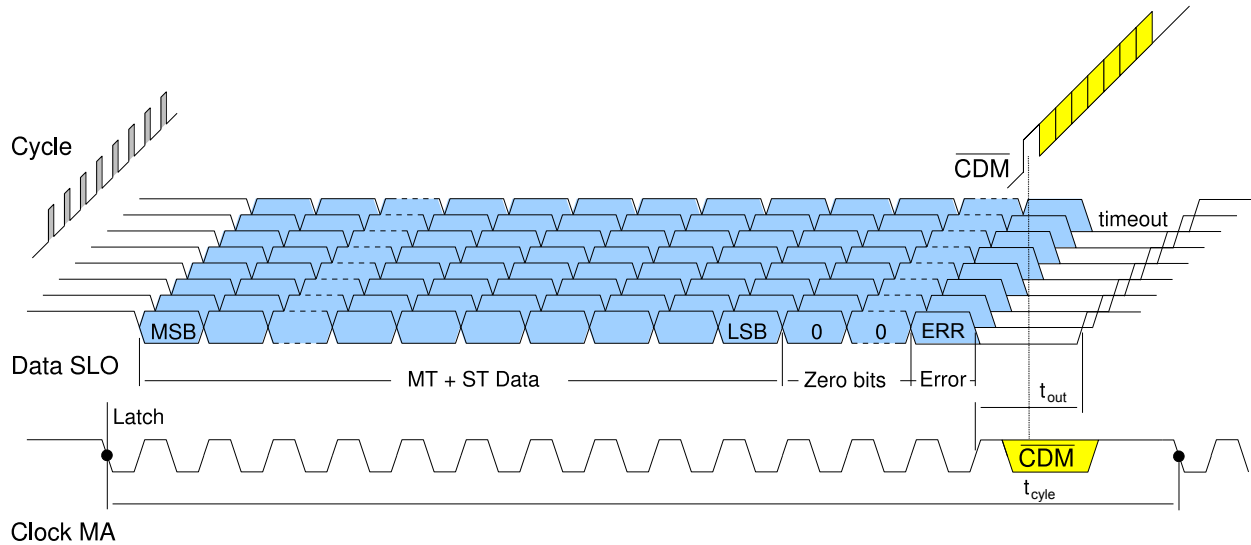


Figure 14: Example of SSI line signals (MODEA=0x5/0x6) with optional unidirectional register communication

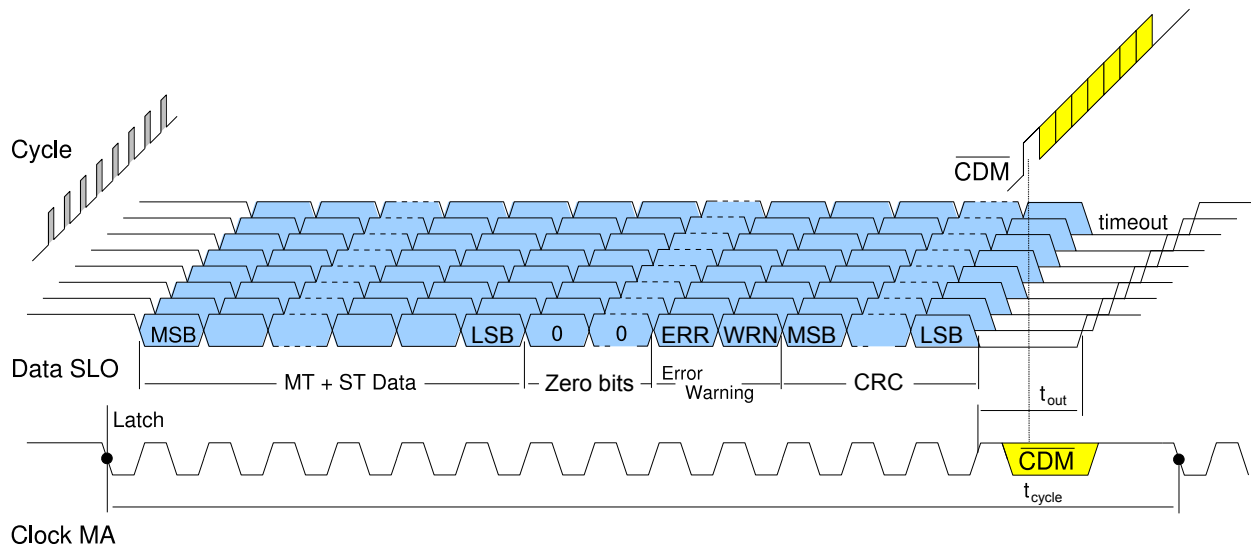


Figure 15: Example of extended SSI line signals (MODEA=0x7, ExtSSI)

MODEA	
Code	Description
0x4	Standard SSI, no error-bit
0x5	Standard SSI, error-bit low active
0x6	Standard SSI, error-bit high active
0x7	extended SSI, data-package like BiSS-C

Table 38: MODEA: SSI

In standard SSI mode singleturn data and, optionally, multiturn data, an error, and a stop zero can be transmitted. In extended SSI mode (ExtSSI) the multiturn data (optional), singleturn data, error, warning, and CRC can be read out. All data is sent with the MSB first and is equivalent to the data package that is output through BiSS.

The SSI interface of iC-MU can handle sensor data communication and unidirectional register communication (Advanced SSI protocol see Figure 14).

In SSI mode the sensor data can be output in binary or Gray code.

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preliminary



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<b>GSSI</b>		Addr. 0x12; bit 7
Code	Data format	
0	binary coded	
1	Gray coded	

Table 39: Data format (for MT and ST data)

<b>RSSI</b>		Addr. 0x12; bit 6
Code	Ring operation	
0	normal output	
1	Ring operation	

Table 40: Ring operation

SSI interface ring operation can either be achieved by externally short-circuiting SLO and SLI or by using parameter RSSI.

## SPI interface: general description

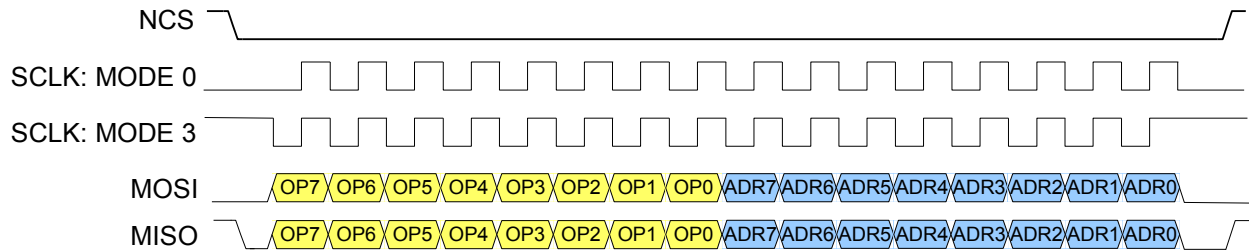


Figure 16: SPI transmission SPI-Mode 0 and 3, using opcode Read REGISTER(single) as an example

MODEA	
Code	Description
0x0	SPI <sub>TRI</sub>
0x1	SPI

Table 41: MODEA: SPI

In mode SPI<sub>TRI</sub> MISO (Pin PA3) is set to tristate if the slave is not selected by the master, i.e. NCS=1.

SPI modes 0 and 3 are supported, i.e. idle level of SCLK 0 or 1, acceptance of data on a rising edge. Data is sent in packages of 8 bits and with the MSB first (see Figure 16). Each data transmission starts with the master sending an opcode (Table 42) to the slave.

The following describes the typical sequence of an SPI data transmission, taking the command **Read REGISTER (single)** as an example (see Figure 16):

1. The master initializes a transmission with a falling edge at NCS.
2. iC-MU passes the level on from MOSI to MISO.
3. The master transmits the opcode OP and address ADR via MOSI; iC-MU immediately outputs OP and ADR via MISO.
4. The master terminates the command with a rising edge at NCS.
5. iC-MU switches its MISO output to 1 (MODEA=0x1) or tristate (MODEA=0x0).

OPCODE	
Code	Description
0xB0	ACTIVATE
0xA6	SDAD-transmission (sensor data)
0xF5	SDAD Status (no latch)
0x97	Read REGISTER(single)
0xD2	Write REGISTER (single)
0xAD	REGISTER status/data

Table 42: SPI OPCODEs

For the setup to be compatible with SPI protocol, when setting the sensor data length for the command "SDAD transmission" with parameters OUT\_MSB, OUT\_LSB, and OUT\_ZERO, it must be ensured that the output data length is a multiple of 8 bits.

## SPI interface: Command ACTIVATE

Each iC-MU has one RACTIVE and one PACTIVE register. These registers are used pairwise to configure the register data channel and the sensor/actuator data channel of a slave.

Using the **ACTIVATE** command, the register and sensor data channels of the connected slaves can be switched on and off. The command causes all slaves to switch their RACTIVE and PACTIVE registers between MOSI and MISO and set them to 0 (slaves in chain connection). The register and sensor/actuator data channels can be switched on and off with data bytes following the OPCODE.

After startup of iC-MU RACTIVE and PACTIVE is set to 1.

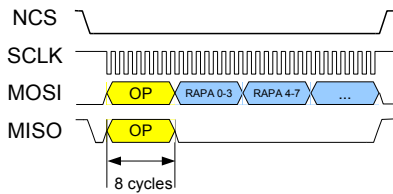


Figure 17: Set ACTIVATE: RACTIVE/PACTIVE (several slaves)

The **ACTIVATE** command resets the bits FAIL, VALID, BUSY, and DISMISS in the SPI-STATUS byte (see Table 46).

RACTIVE	
Code	Description
0	Register communication deactivated
1	Register communication activated*)
Note	*) default after startup

Table 43: RACTIVE

If RACTIVE is not set, on commands **Read REGISTER (single)**, **Write REGISTER (single)**, **REGISTER status/data** the ERROR bit is set in the SPI-STATUS byte (see Table 46) to indicate that the command has not been executed. At MISO the slave immediately outputs the data transmitted by the master via MOSI.

PACTIVE	
Code	Description
0	Sensor data channel deactivated
1	Sensor data channel activated*)
Note	*) default after startup

Table 44: PACTIVE

If PACTIVE is not set, on commands **SDAD status** and **SDAD transmission** the ERROR bit is set in the SPI-STATUS byte (see Table 46) to indicate that the command has not been executed. At MISO the slave immediately outputs the data transmitted by the master via MOSI.

If only one slave is connected up with one register and one sensor data channel, it must be ensured that the RACTIVE and PACTIVE bits come last in the data byte.

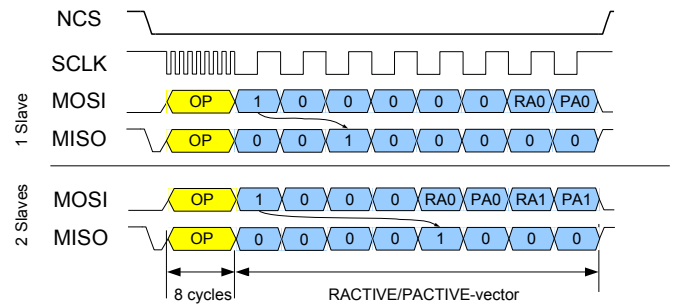


Figure 18: Set ACTIVATE: RACTIVE/PACTIVE (Example with one and two slaves)

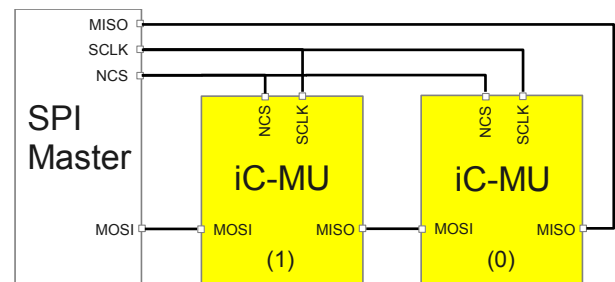


Figure 19: Example configuration with 2 Slaves (daisy chained)

### SPI interface: Command SDAD transmission

iC-MU samples the actual converter values on the first rising edge at SCLK, when NCS is at zero (REQ). Because iC-MU can output the sensor data (SD) immediately, the master can transmit the **SDAD transmission** command directly. The sensor data shift register (the size of which is 8 to 40 bits in multiples of 8 using iC-MU) is switched and clocked out between MOSI and MISO.

If invalid data is sampled in the shift register, the ERROR bit is set in the SPI-STATUS byte (see Table 46) and the output data bytes are set to zero.

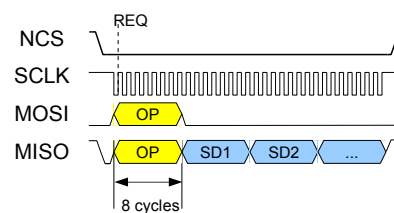


Figure 20: SDAD transmission: read SD

### SPI interface: Command SDAD status

If the master does not know the processing time of the connected slaves, it can request sensor data using the command **SDAD status**. The command causes:



1. All slaves activated via PACTIVE to switch their SVALID register between MOSI and MISO.
2. The next request for sensor data started with the first rising edge at SCLK of the next SPI communication is ignored by the slave.

The end of conversion is signaled by SVALID (SV). Using this command, the master can poll to the end of conversion. The sensor data is read out via the command **SDAD transmission**.

SVALID	
Code	Description
0	Sensor data invalid
1	Sensor data valid

Table 45: SVALID

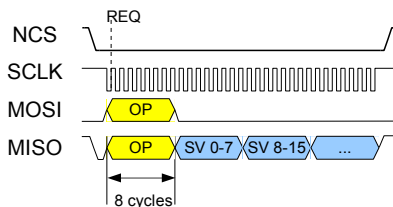


Figure 21: SDAD status

If only one slave is connected, the corresponding SVALID bit (SV0) is placed at bit position 7 in the SVALID byte.

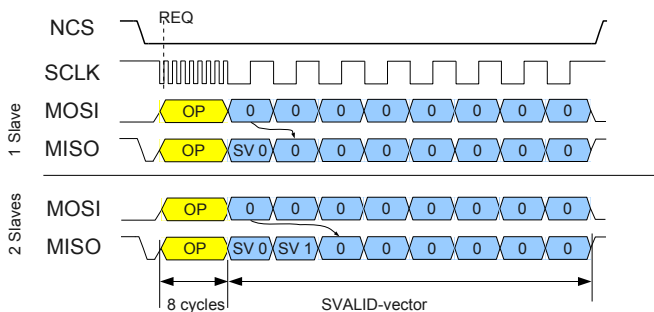


Figure 22: SDAD status (Example with one and two slaves)

Picture 23 shows the interaction of the two commands **SDAD Status** and **SDAD transmission**. It is not necessary to start each sensor data communication with the command **SDAD Status** (1). iC-MU has no processing time and can therefore directly output valid sensor data. Because of that the command sequence can start with **SDAD-transmission** (2). Following this, the command **REGISTER status/data** should be executed to detect an unsuccessful SPI communication.

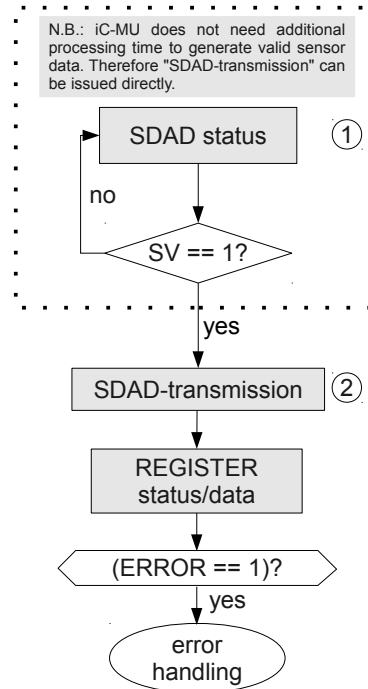


Figure 23: Example sequence of the commands SDAD Status/SDAD-transmission

### SPI interface: Command Read REGISTER (single)

This command enables register data to be read out from the slave byte by byte.

The master first transmits the **Read REGISTER (single)** command and then address ADR. The slave immediately outputs the command and address at MISO.

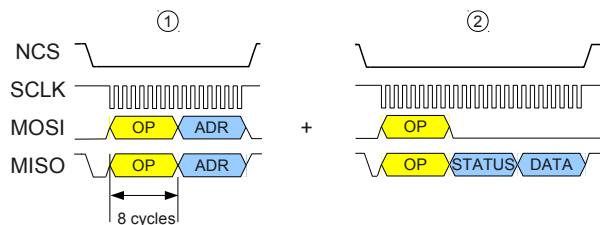


Figure 24: Read REGISTER (single): set the read address (1) + command REGISTER status/data to read-out data (2)

Following this, using the **REGISTER status/data** command (see page 34) the master can poll until the validity of the DATA following the SPI-STATUS byte is signaled via SPI-STATUS.

### SPI interface: Command Write REGISTER (single)

This command enables data to be written to the slave byte by byte.

The master first transmits the **Write REGISTER (single)** command and then address ADR and the data (DATA). The slave immediately outputs the command, address, and data at MISO.

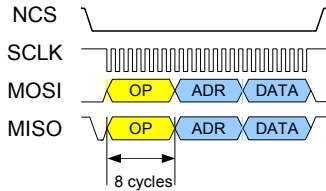


Figure 25: Write REGISTER (single); set WriteAddress and Data

Using the **REGISTER status/data** command, the master can poll to the end of communication (signaled via the SPI-STATUS byte).

### SPI interface: Command REGISTER status/data

The **REGISTER status/data** command can be used to request the status of the last register communication and/or the last data transmission. The SPI-STATUS byte contains the information summarized in Table 46.

SPI-STATUS		
Bit	Name	Description of the status report
7	ERROR	Opcode not implemented, Sensor data was invalid on readout
6..4	-	Reserved
Statusbits of the register communication		
3	DISMISS	Address refused
2	FAIL	Data request has failed
1	BUSY	Slave is busy with a request
0	VALID	DATA is valid
Note	Display logic: 1 = true, 0 = false	

Table 46: Communication status byte

All SPI status bits are updated with each register access. The exception to the rule is the ERROR bit; this bit indicates whether an error occurred during the last SPI-communication with the slave.

The master transmits the **REGISTER status/data** opcode. The slave immediately passes the opcode on to MISO. The slave then transmits the SPI-STATUS byte and a DATA byte.

Following the commands **Read REGISTER (single)** and **Write REGISTER (single)**, the validity of the DATA byte is signaled with the VALID status bit.

The requested data byte is returned via DATA following the **Read REGISTER (single)** command. Following the **Write REGISTER (single)** command, the data to be written is repeated in the DATA byte. With all other opcodes, the DATA byte is not defined.

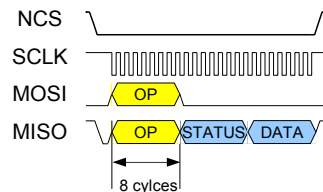


Figure 26: REGISTER status/data

Figure 27 shows the interaction of the commands **REGISTER read/write** and **REGISTER status/data**.

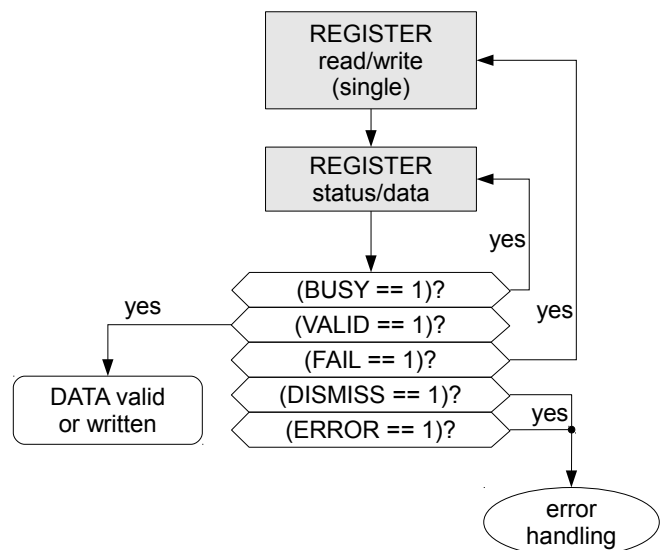


Figure 27: Example sequence of commands REGISTER read/write and REGISTER status/data

## CONVERTER AND NONIUS CALCULATION

### Converter principle

The system consist of two real-time tracking converters, each with a resolution of 12 bits for the master track and nonius track. Above the maximal permissible input frequency the status bits FRQ\_CNV is set. The tracking converter can't follow the input signal any more. With a filter setting of type FILT1 and bigger an increased resolution of 14 bits is available.

A digital filter can be configured with FILT to reduce the noise of the digital output signals. Using this the digital angle values of the tracking converter can be filtered.

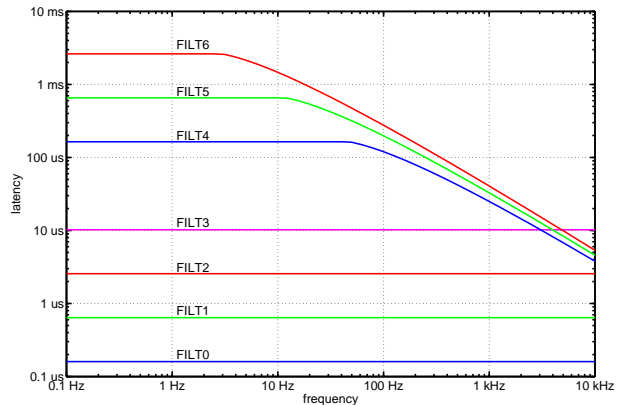


Figure 29: Filter latencies

FILT Addr. 0x0E; bit 2:0			
Code	Type	noise sup-pression	latency
0x0	FILT0	0 dB	< 1 μs
0x1	FILT1	15 dB	< 1 μs
0x2	FILT2	21 dB	2.5 μs
0x3	FILT3	27 dB	10 μs
0x4	FILT4	39 dB	164 μs $f_{sin} < 50 \text{ Hz}$ 25 μs $f_{sin} < 1 \text{ kHz}$
0x5	FILT5	45 dB	650 μs $f_{sin} < 12 \text{ Hz}$ 33 μs $f_{sin} < 1 \text{ kHz}$
0x6	FILT6	51 dB	2.6 ms $f_{sin} < 3 \text{ Hz}$ 41 μs $f_{sin} < 1 \text{ kHz}$

Table 47: Digital filter features

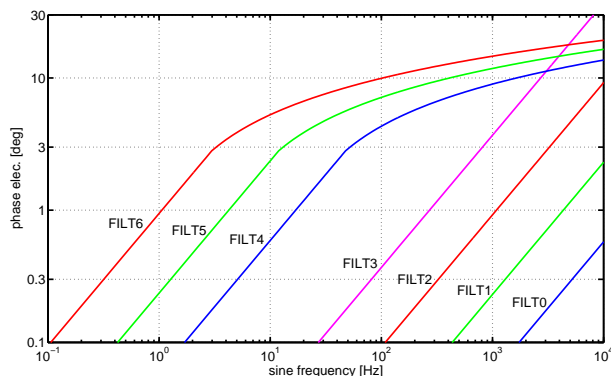


Figure 28: Phase relationship of the filters

### Synchronization mode

Table 48 lists the configurable master period counts and the resulting bit lengths for nonius synchronization, and the synchronization bit length used. The paramter MPC defines thus the nonius system and has to be chosen according to the magnetic code carrier. If MPC is switched during operation, command ABS\_RESET must be executed and the track offset values must be calibrated again.

MPC(3:0) Addr. 0x0F; bit 3:0				
Code	Master period count	Nonius period count	bitlength	synchroni-sation bitlength
0x4	16	15	4	8
0x5	32	31	5	7
0x6	64	63	6	6
for MU as Nonius-Multiturn *)				
0x7	128	127	7	5
0x8	256	255	8	4
0x9	512	511	9	3
0xA	1024	1023	10	2
0xB	2048	2047	11	1
0xC	4096	4095	12	0
Note	*) see page 40			

Table 48: Master period count and the resulting bit lengths

LIN selects the hall sensors for linear or rotative systems.

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LIN		Addr. 0x0E; bit 4
Code	Description	
0	Rotative	
1	Linear	

Table 49: Selection of linear/rotative hall sensors

An offset between the nonius track and the master track within one revolution can be adjusted with SPO\_BASE and SPO\_x (x=0-14) .

The following formula describes how the error curve based on the raw data from the master and nonius track can be calculated. MPC is the number of sine periods of the measuring distance.

$$TOL_{SPON} = RAW_{MASTER} - RAW_{NONIUS} * \frac{2^{MPC}}{2^{MPC} - 1}$$

The maximum tolerable phase deviation for a 2-track nonius system is shown in Table 50. For the tolerable phase deviation of a 3-track nonius system please refer to Table 64 page 40.

Periods/revolution		Permissible Max. Phase Deviation [given in degree per signalperiod of 360°] Master ↔ Nonius
Master	Nonius	
16	15	+/- 9.84°
32	31	+/- 4.92°
64	63	+/- 2.46°

Table 50: Tolerable phase deviation for the master versus the nonius track of a 2 track nonius system (with reference to 360°, electrical)

An offset correction curve can be specified with SPO\_BASE and SPO\_x (x = 0-14). SPO\_BASE is the start-value. SPO\_0 to SPO\_14 can be interpreted as slope-values. A change in the slope of the offset function can be made each 22.5°. The slope value SPO\_15 is computed automatically by iC-MU. To do this the following condition must be met:

$$\sum_{x=0}^{14} SPO\_x = \{-7 \dots 7\}$$

The offset value between to slopes (e.g. SPO\_0 and SPO\_1) is interpolated. The computed offset is added to the converted result of the nonius track prior to synchronization and is used to calibrate the nonius to the master track. An offset value is chosen by the absolute position given by the nonius difference (master-nonius).

SPO_BASE(3:0)		Addr. 0x19; bit 3:0
SPO_BASE(3:0)		Addr. SER:0x52; bit 3:0
Code	Starting point referred to 1 revolution	
0x0	0 * (22.5° / 2 <sup>MPC</sup> )	
...	...	
0x7	7 * (22.5° / 2 <sup>MPC</sup> )	
0x8	-8 * (22.5° / 2 <sup>MPC</sup> )	
0x9	-7 * (22.5° / 2 <sup>MPC</sup> )	
...	...	
0xF	-1 * (22.5° / 2 <sup>MPC</sup> )	

Table 51: Nonius track offset start value

<b>SPO_0(3:0)</b>	Addr. 0x19; bit 7:4	Addr. SER: 0x52
<b>SPO_1(3:0)</b>	Addr. 0x1A; bit 3:0	Addr. SER: 0x53
<b>SPO_2(3:0)</b>	Addr. 0x1A; bit 7:4	Addr. SER: 0x53
<b>SPO_3(3:0)</b>	Addr. 0x1B; bit 3:0	Addr. SER: 0x54
<b>SPO_4(3:0)</b>	Addr. 0x1B; bit 7:4	Addr. SER: 0x54
<b>SPO_5(3:0)</b>	Addr. 0x1C; bit 3:0	Addr. SER: 0x55
<b>SPO_6(3:0)</b>	Addr. 0x1C; bit 7:4	Addr. SER: 0x55
<b>SPO_7(3:0)</b>	Addr. 0x1D; bit 3:0	Addr. SER: 0x56
<b>SPO_8(3:0)</b>	Addr. 0x1D; bit 7:4	Addr. SER: 0x56
<b>SPO_9(3:0)</b>	Addr. 0x1E; bit 3:0	Addr. SER: 0x57
<b>SPO_10(3:0)</b>	Addr. 0x1E; bit 7:4	Addr. SER: 0x57
<b>SPO_11(3:0)</b>	Addr. 0x1F; bit 3:0	Addr. SER: 0x58
<b>SPO_12(3:0)</b>	Addr. 0x1F; bit 7:4	Addr. SER: 0x58
<b>SPO_13(3:0)</b>	Addr. 0x20; bit 3:0	Addr. SER: 0x59
<b>SPO_14(3:0)</b>	Addr. 0x20; bit 7:4	Addr. SER: 0x59
Code	Slope referred to 1 revolution	
0x0	0 * (22.5° / 2 <sup>MPC</sup> )	
...	...	
0x7	7 * (22.5° / 2 <sup>MPC</sup> )	
0x8	-8 * (22.5° / 2 <sup>MPC</sup> )	
0x9	-7 * (22.5° / 2 <sup>MPC</sup> )	
...	...	
0xF	-1 * (22.5° / 2 <sup>MPC</sup> )	
Note	$\sum_{x=0}^{14} SPO\_x = \{-7 \dots 7\} * (22.5° / 2^{MPC})$	

Table 52: Nonius track offset slopes

SPO_15(3:0)		Addr. SER:0x5A; bit 3:0
Code	Slope	
0x0	-	
...	is automatically computed: $-\sum_{x=0}^{14} SPO\_x$	
0xF	-	
Note	internal register, not readable via serial interface	

Table 53: Nonius track offset slope (is automatically computed)

The principle is shown in Figure 30. The red curve corresponds to the error curve of the nonius difference absolute within 360°. By taking the blue marked SPO\_x curve it is shown, that the nonius difference can be changed in a way that the resulting green curve is in the valid synchronisation range. It can be seen that

an error within 22.5° (in the Figure between 67.5° and 90°) can not be corrected. For SPO\_0 the range of a possible slope change is exemplary shown.

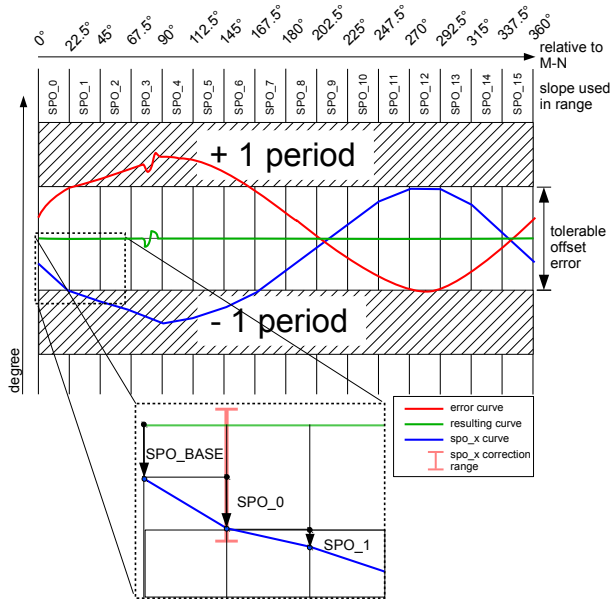


Figure 30: Nonius track offset calibration

Following the first nonius synchronization the number of excessed periods is counted and output. Using NCHK\_NON the system can be configured to check the internal period counter against the period given by the code disc at regular intervals. Command NON\_VER explicitly requests nonius verification. If an error is found during verification of the nonius, bit NON\_CTR is set in status register STATUS1.

Figure 31 describes the principle of nonius synchronization with verification, with  $\varphi$  representing the respective digitized angle of the relevant track.

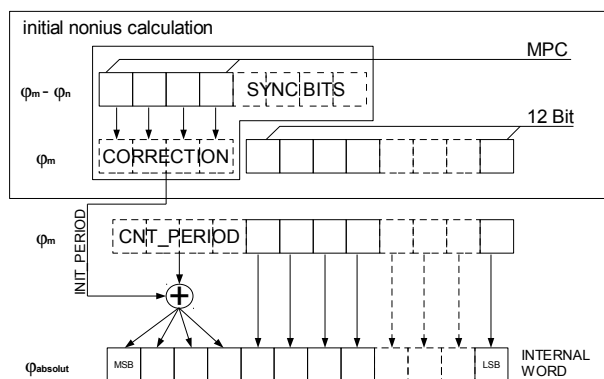


Figure 31: Principle of nonius synchronization

NCHK_NON Addr. 0x0D; bit 5	
Code	Description
0	automatic period verification
1	no automatic period verification

Table 54: Automatic nonius period verification

The nonius data and incremental interface can be automatically reset with ACRM\_RES if the master amplitude is too low. The incremental section is reset as soon as the amplitude control unit indicates that the master amplitude is too low (AM\_MIN occurs, see Table 91). The ABZ-interface shows position 0 as default. When the master amplitude is again in its set range, a new nonius calculation is carried out and the incremental section is restarted.

ACRM_RES Addr. 0x0D; bit 4	
Code	Description
0	no automatic reset
1	automatic reset active

Table 55: Automatic Reset triggered by AM\_MIN

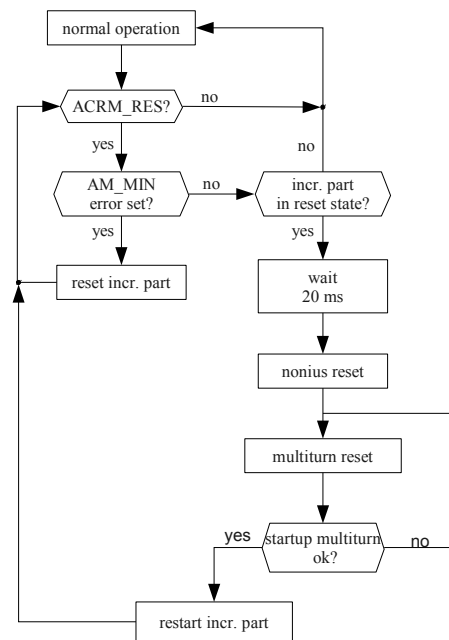


Figure 32: Automatic reset ACRM\_RES

## MT INTERFACE

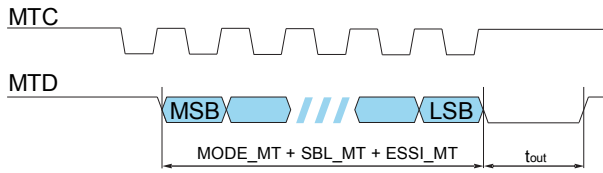


Figure 33: Example of multiturn SSI line signals

### Configuration of the Multiturn interface

iC-MU can read in and synchronize binary data from an external SSI sensor through the serial multiturn interface. On startup the first data value read in determines the start value of the internal period counter. After startup the multiturn periods are counted internally and output. If there is an error reading the multiturn during startup, the read-in will be repeated.

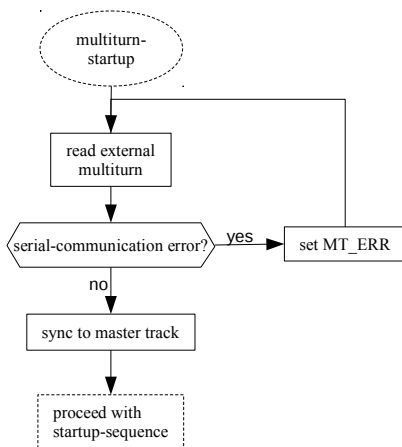


Figure 34: Error handling during startup

If the MT interface is not used (MODE\_MT=0x0), the internal 24-bit period counter can extend the singleturn data output to include the counted multiturn cycles.

For exclusive multiturn systems a 4, 8, 12, 16 or 18-bit multiturn data value can be read in (MODE\_MT=0xB-0xE). There is also the possibility to interpret a part of the external multiturn data value as singleturn. For further information see **Construction of a Multiturn system with two iC-MU S. 40.**

MODE_MT(3:0) Addr. 0x10; bit 3:0			
Code	Function	Code	Function
0x0	no external data	0x8	4 *) + 12 bit
0x1	1 *) bit	0x9	5 *) + 12 bit
0x2	2 *) bit	0xA	6 *) + 12 bit
0x3	3 *) bit	0xB	4 bit
0x4	4 *) bit	0xC	8 bit
0x5	5 *) bit	0xD	12 bit
0x6	6 *) bit	0xE	16 bit
0x7	3 *) + 12 bit	0xE	18 bit
Notes:	*) data interpreted as ST If MPC ≥ 0x07 than MODE_MT has to be set to 0x0 or 0xD		

Table 56: MT interface operating mode

For synchronization a synchronization bit length must be set by SBL\_MT. Synchronization takes place between the read external multiturn word and the internal counted cycle data. Synchronization can take place automatically within the relevant phase tolerances.

SBL_MT(1:0) Addr. 0x10; bit 5:4		
Code	MT synchronisation bitlength	synchronisation tolerance (ST-resolution)
0x0	1 bit	± 90°
0x1	2 bit	± 90°
0x2	3 bit	± 135°
0x3	4 bit	± 157,5°

Table 57: MT synchronization bit length

Figure 35 shows the principle of a 2 bit MT synchronization for ideal signals (without indication of synchronization tolerance limits).

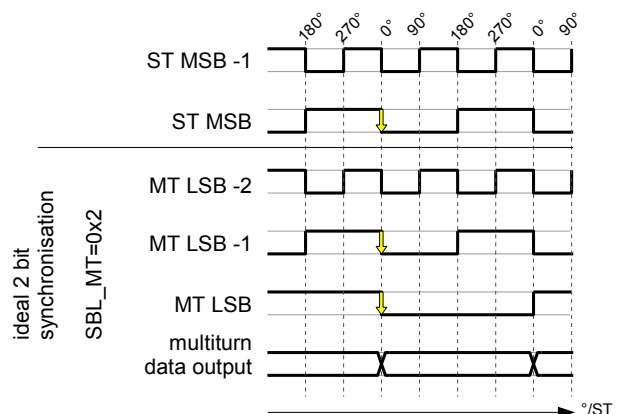


Figure 35: Principle of 2 bit MT synchronization

The direction of rotation of the read multiturn data can be inverted using parameter ROT\_MT.

ROT_MT		Addr. 0x0E; bit 5
Code	Function	
0	no inversion of direction of rotation	
1	inversion of direction of rotation	

Table 58: Inverted direction of rotation of external multiturn

The parameter ESSI\_MT configures the evaluation of an optional error-bit send by the external multiturn device.

ESSI_MT		Addr. 0x0E; bit 7:6
Code	Function	
0x0	no error bit	
0x1	1 error-bit low active	
0x2	reserved	
0x3	1 error-bit high active	

Table 59: Evaluation of an error-bit of the external multiturn

The total data length of the external read multiturn data word is determined by:

$$\text{data\_length\_ext\_mt} = \text{Bits}(\text{MODE\_MT}) + \text{Bits}(\text{SBL\_MT}) + \text{Bits}(\text{ESSI\_MT})$$

The parameter SPO\_MT allows to balance an existing static offset between the singleturn and the multiturn. The offset is added before the synchronization of the read multiturn data (see Figure 36).

SPO_MT		Addr. 0x0F; bit 7:4
Code	Function	
0x0	...	
...	multiturn offset	
0xF	...	

Table 60: Offset of external multiturn

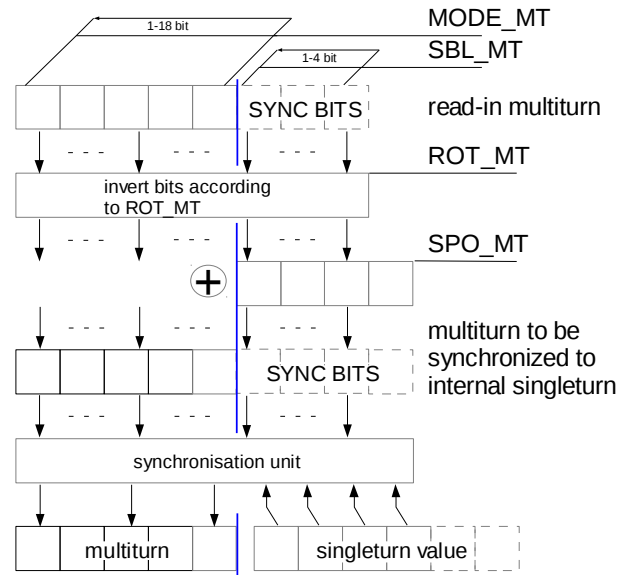


Figure 36: Parameters to configure external multiturn

CHK\_MT can be used to verify the counted multiturn at regular intervals. Verification can also be requested using command MT\_VER. A multiturn verification error (comparison of the internal counted multiturn cycles with the external multiturn data) is signaled through the status bit MT\_CTR.

CHK_MT		Addr. 0x10; bit 6
Code	Function	
0	no verification	
1	periodical verification	

Table 61: Multiturn verification

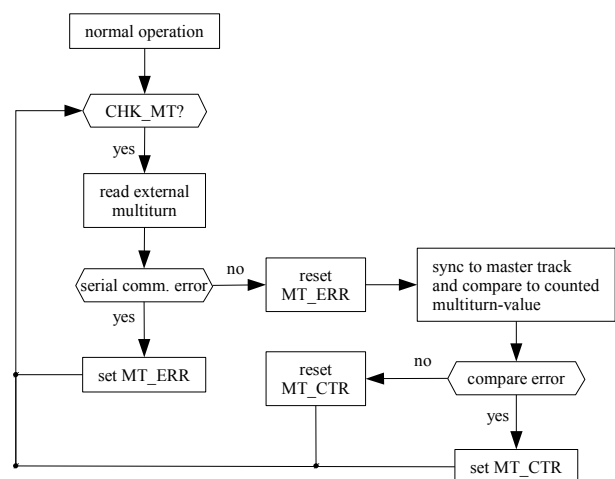


Figure 37: Error handling in normal operation with cyclic verification of the period counter

# iC-MU OFF-AXIS NONIUS ENCODER WITH INTEGRATED HALL SENSORS

## Construction of a Multiturn system with two iC-MU

A 3 Track nonius system can be build using two iC-MU. The singleturn iC-MU (1) can be configured to interpret 3, 4, 5, or 6 bits of the read multiturn data as singleturn data (ST) (see Table 56). The output through the incremental interface of iC-MU (1) is then absolute with this additional information.

The construction of such a system is shown as an example in Figure 38 and the configuration in Table 62.

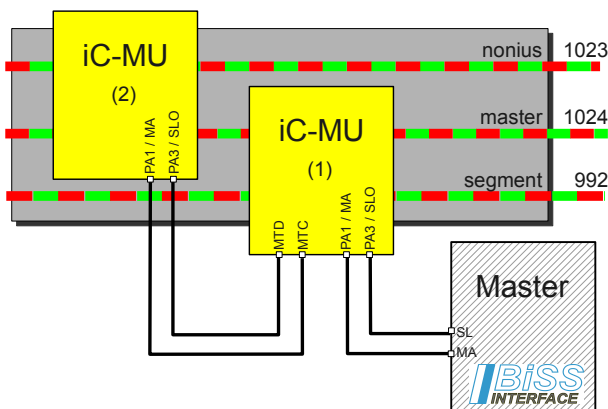


Figure 38: 3-track nonius with 2 iC-MU

iC-MU (1): singleturn		
Parameter	Value	Description
MPC	0x5	5 Bit ST periods
MODE_MT	0x5	5 Bit ST periods via multiturn
SBL_MT	0x3	4 Bit synchronisation of read multiturn data
iC-MU (2): multiturn		
Parameter	Value	Description
MPC	0xA	10 Bit periods
MODE_MT	0x0	no additional multiturn data
MODE_ST	0x0	output of internal absolute data
OUT_MSB	0xA	MSB output configuration 9 Bit output data while having 10 Bit periods
OUT_LSB	0xF	LSB output configuration 9 Bit output data while having 10 Bit periods

Table 62: Configuration example for the 3-track nonius system of Fig.38

Table 63 shows the possible settings for a 3-track nonius systems with 2 iC-MU and the resulting periods/revolution of the tracks. The maximum phase deviation of the tracks is summarized in Table 64.

MPC (2)	(1)	Periods/revolution			ST Periods [Bit]	
		Master	Segm.	Nonius	from MT(2)	from ST(1)
0x7	0x4	128	120	127	3	4
0x8	0x4	256	240	255	4	4
0x9	0x5	512	496	511	4	5
0xA	0x5	1024	992	1023	5	5
0xB	0x6	2048	2016	2047	5	6
0xC	0x6	4096	4032	4095	6	6

Table 63: Settings for a 3-track nonius system using 2 iC-MU

Periods/revolution Master	Segm.	Nonius	Permissible Max. phase deviation [given in degree per signalperiod of 360°]	
			Master ↔ Segm. (1)	Master ↔ Non.* (2)
128	120	127	+/-9.84°	+/-19.68°
256	240	255	+/-9.84°	+/-9.84°
512	496	511	+/-4.92°	+/-9.84°
1024	992	1023	+/-4.92°	+/-4.92°
2048	2016	2047	+/-2.46°	+/-4.92°
4096	4032	4095	+/-2.46°	+/-2.46°
Note	*) with SBL_MT=0x3			

Table 64: Tolerable phase deviation for the master versus the nonius or segment track of a 3-track nonius system (with reference to 360°, electrical)

Figure 39 shows the principle of the synchronisation of the data from iC-MU (2) to iC-MU (1).

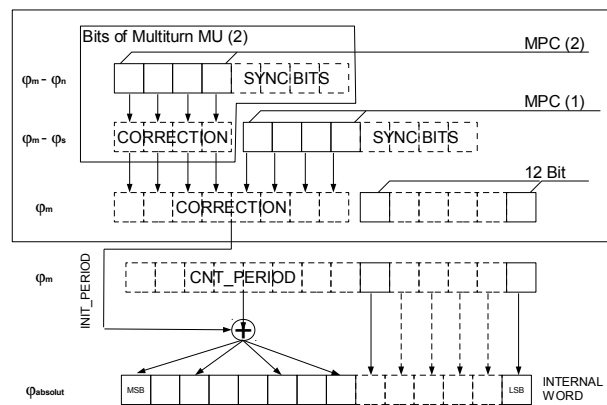


Figure 39: Principle of the synchronisation of a 3-track nonius system using 2 iC-MU without further multiturn data

To facilitate the initial configuration of an iC-MU as a SSI multiturn device the command SWITCH can be used (see page 52). The singleturn iC-MU (1) in Figure 38 has to enable the direct communication to the multiturn sensor by setting GET\_MT to 1. The configuration of iC-MU (2) can take place using the BiSS protocol. After the configuration of the external multiturn MODEA\_NEW and RPL\_NEW are used



to set the target configuration of MODEA and RPL. After that the command SWITCH is executed. By reading STATUS1 it is possible to control if there was an error while executing the command. After the next startup or after the execution of the command SOFT\_RESET iC-MU starts with the interface configured with MODEA\_NEW and RPL\_NEW.

## Direct Communication To Multiturn Sensor

Making use of the BiSS Interface bus capabilities, iC-MU can connect in modes MODEA = 0x02 and 0x04-0x07 (BiSS and SSI) the external multiturn sensor to the BiSS master controller when GET\_MT is enabled. To this end pin MA (PA1) receiving the BiSS master's clock signal is fed through to pin MTC and the MTD pin is activated in place of the SLI (PA2) pin. Upon enabling this mode the single cycle timeout must have

elapsed and an additional init command carried out by the BiSS master, before it can run the first register communication.

Example: external multiturn sensor built with iC-MU is connected to the MT interface of a first iC-MU, preparing the singleturn data. With GET\_MT enabled, the external multiturn can then be addressed via BiSS ID 0 and the singleturn via BiSS ID 1. This temporal chain operation simplifies device parametrization during encoder manufacturing.

GET_MT		Addr. 0x10; bit 7
Code	Function	
0	Disabled	
1	MT sensor communication enabled	

Table 65: Direct BiSS communication enable for MT sensor via I/O Interface

## INCREMENTAL OUTPUT ABZ, STEP/DIRECTION AND CW/CCW

MODEA	
Code	Description
0x3	ABZ
MODEB	
Code	Description
0x0	ABZ
0x2	Step/Direction
0x3	CW/CCW Incremental
Notes:	It is not possible to select an incremental interface on MODEA and MODEB simultaneously

Table 66: MODEA/MODEB: ABZ, step/direction and CW/CCW

The resolution of incremental signals ABZ can be programmed for each singleturn cycle within a range of 4 to 262,144 edges using the internal FlexCount®. The number of master periods which is equivalent to a singleturn cycle is defined by the settings in register MPC (Table 48).

RESABZ(7:0)	Addr. 0x13; bit 7:0	
RESABZ(15:0)	Addr. 0x14; bit 7:0	
Code	Resolution	Interpolation factor
0x0000	4	1
0x0001	8	2
...	...	...
0xFFFF	262144	65536
Notes:	For non-binary resolutions above 32,768 (0x2000) the relative error increases	

Table 67: FlexCount®- Resolution

Figure 40 shows the ABZ, step/direction, and CW/CCW signals. The length of a signal A or B cycle is defined by  $\varphi_{360AB}$  as a range between two rising edges of an A or B signal.

$\varphi_{hys}$  represents the hysteresis which must be exceeded before further edges are generated at the incremental interface.

Minimum edge distance  $t_{mtd}$  is the minimum time which must have elapsed before another event can be output at the incremental interface.

The length of the Z pulse with setting ZLEN = 0x00 is defined by  $\varphi_{z90}$ .

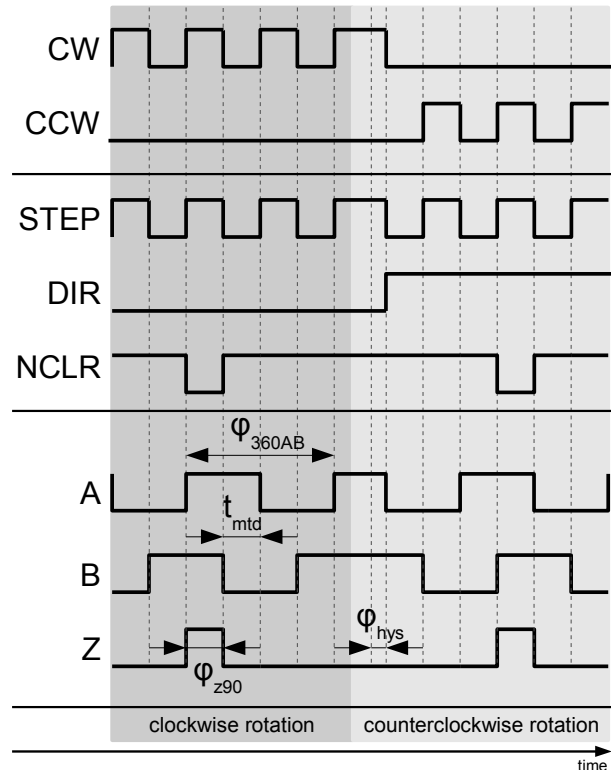


Figure 40: Definition of the ABZ, STEP/DIR, and CW/CCW signals

The phase position of the incremental output signals can be inverted using the relevant configuration bit INV\_x (x = A,B,Z).

INV_A		Addr. 0x16; bit 2
Code	A/STEP/CW-Signal	
0	normal	
1	inversion	

Table 68: Inversion A-Signal

INV_B		Addr. 0x16; bit 1
Code	B/DIR/CCW-Signal	
0	normal	
1	inversion	

Table 69: Inversion B-Signal

INV_Z		Addr. 0x16; bit 0
Code	Z/NCLR-Signal	
0	normal	
1	inversion	

Table 70: Inversion Z-Signal

Index pulse Z can be programmed in four lengths. The position of the index pulse in relation to the A/B signals is shown in Figure 41.

LENZ(1:0) Addr. 0x16; bit 7:6	
Code	Z-pulse length
0x0	90°
0x1	180°
0x2	270°
0x3	360°

Table 71: Index pulse length

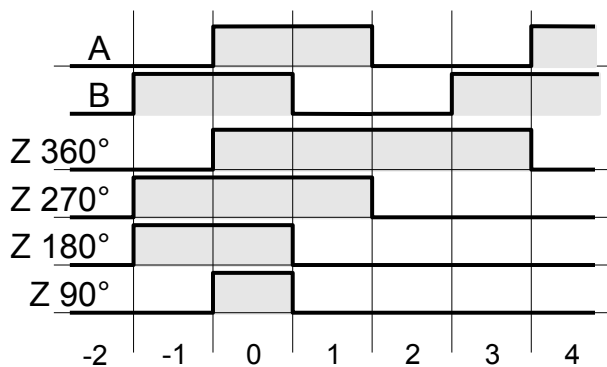


Figure 41: Index pulse length settings

The direction of rotation can be inverted with parameter ROT. The parameter affects the output of the data word through the serial interface in MODE\_ST=0x0 and 0x1, the ABZ-interface and the UVW-interface.

ROT Addr. 0x15; bit 7	
Code	Description
0	no inversion of direction of rotation
1	inversion of rotation

Table 72: Inverted direction of rotation

Parameter SS\_AB must be configured depending on the maximum speed. With a filter setting of FILT = 0x00 (Table 47), correspondingly higher SS\_AB step size values must be programmed. The maximum possible resolution of the incremental count signal is reduced according to the set step size. The FRQ\_ABZ status bit is set in the case of an unacceptable high speed.

SS_AB(1:0) Addr. 0x15; bit 5:4		
Code	max. resolution	max. rpm
0x0	2 <sup>18</sup>	6000 rpm
0x1	2 <sup>17</sup>	12000 rpm
0x2	2 <sup>16</sup>	6000 rpm mit FILT=0x0
0x3	2 <sup>15</sup>	12000 rpm mit FILT=0x0

Table 73: System AB step size

The minimum edge distance  $t_{mtd}$  of the ABZ, STEP/DIR or CW/CCW interface can be limited by setting the maximum output frequency with FRQAB. It can be used to adjust the output frequency to a frequency limit given by an external ABZ, STEP/DIR or CW/CCW counter device.

FRQAB(2:0) Addr. 0x15; bit 2:0		
Code	Output frequency AB	Edge distance $t_{mtd}$
0x0	6.25 MHz	40 ns
0x1	3.13 MHz	80 ns
0x2	1.56 MHz	160 ns
0x3	781.25 kHz	320 ns
0x4	390.63 kHz	640 ns
0x5	195.31 kHz	1.28 $\mu$ s
0x6	48.83 kHz	5.12 $\mu$ s
0x7	12.2 kHz	20.48 $\mu$ s

Table 74: AB output frequency

The incremental counter has an integrated hysteresis which prevents multiple switching of the incremental signals at the reversing point. Hysteresis  $\varphi_{hys}$  must first be exceeded before edges can again be generated at A or B. This hysteresis can be set within a range of 0° to 0.35° according to Table 75 and is referenced to 360° of a singleturn cycle.

CHYS_AB(1:0) Addr. 0x16; bit 5:4	
Code	Hysteresis
0x0	no hysteresis
0x1	0.175°
0x2	0.35°
0x3	0.7°

Table 75: Hysteresis with an inverted direction of rotation

The parameter ENIF\_AUTO selects whether at startup the incremental interface is enabled after the converter has found its operating point or if the counting to the absolute angle can be seen at the incremental interface.

ENIF_AUTO Addr. 0x15; bit 4	
Code	Description
0	counting to operating point visible
1	counting to operating point not visible

Table 76: Incremental interface enable

See the chapter on the preset function (p. 56) to set the offset for ABZ output.

## UVW COMMUTATION SIGNALS

MODEB	
Code	Description
0x1	UVW

Table 77: MODEB: UVW

iC-MU can generate commutation signals for BLDC motors from 1 up to 16 pole pairs. The hysteresis is set fixed to 0.0879° referenced to a mechanical revolution.

Figure 42 shows the commutation sequence for a motor with 6 pole pairs. Here, a commutation sequence spanning an angle of  $\varphi_{360UVW}$  repeats itself 6 times within one mechanical revolution of the motor. The phaseshift between the commutation signals is 120°.

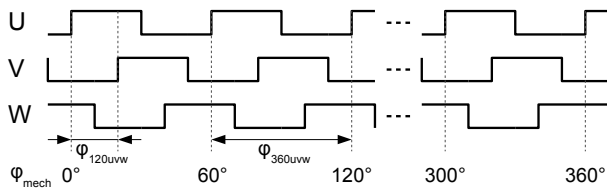


Figure 42: commutation signals UVW

Using parameter PPUVW the number of commutation sequences per mechanical revolution can be set.

PPUVW(5:0) Addr. 0x17; bit 5:0			
Code	number of pole pairs	Code	number of pole pairs
0x02	1 pole pair	0x1A	9 pole pairs
0x05	2 pole pairs	0x1D	10 pole pairs
0x08	3 pole pairs	0x20	11 pole pairs
0x0B	4 pole pairs	0x23	12 pole pairs
0x0E	5 pole pairs	0x26	13 pole pairs
0x11	6 pole pairs	0x29	14 pole pairs
0x14	7 pole pairs	0x2C	15 pole pairs
0x17	8 pole pairs	0x2F	16 pole pairs

Table 78: Number of commutation signal pole pairs

The sequence of the commutation signals can be selected by  $\varphi_{120UVW}$  as in Figure 42 or with a distance of 60° between two neighboring rising edges referenced to one UVW cycle using parameter PP60UVW.

PP60UVW Addr. 0x16; bit 3	
Code	Phase UVW Signale
0	120° phase shift
1	60° phase shift

Table 79: Commutation signal phase length

Register OFF\_UVW is used to set the start angle and compensate for the offset between the winding of the BLDC and the Hall sensor signals. This angle can be set with 12 bits.

### N.B.:

After startup or the commands SOFT\_RESET and ABS\_RESET the OFF\_UVW values are amended to include the nonius data, with a configured multi-turn updated with the multturn data, and stored as OFF\_COM in the internal RAM.

OFF_UVW(3:0) Addr. 0x28; bit 7:4	
OFF_UVW(11:4) Addr. 0x29; bit 7:0	
OFF_UVW(3:0) Addr. SER:0x4B; bit 7:4	
OFF_UVW(11:4) Addr. SER:0x4C; bit 7:0	
Code	Offset UVW signals
0x000	0.00° mech
0x001	0.09° mech
...	$\frac{360.0^\circ \text{ mech}}{4096} \cdot \text{OFF\_UVW}$
0xFFFF	359.9° mech

Table 80: Commutation signal start angle

OFF_COM(3:0) Addr. SER:0x23; bit 7:4		R
OFF_COM(11:4) Addr. SER:0x24; bit 7:0		R
Code	Description	
0x000	start angle commutation signal (automatically computed)	
...		
0xFFFF		

Table 81: Commutation signal start angle amended by the nonius/MT

The direction of rotation can be inverted with parameter ROT. The parameter affects the output of the data word through the serial interface in MODE\_ST=0x0 and 0x1, the ABZ-interface and the UVW-interface.

ROT Addr. 0x15; bit 7	
Code	Description
0	no inversion of direction of rotation
1	inversion of rotation

Table 82: Inverted direction of rotation

## REGISTER ACCESS THROUGH SERIAL INTERFACE (SPI AND BISS)

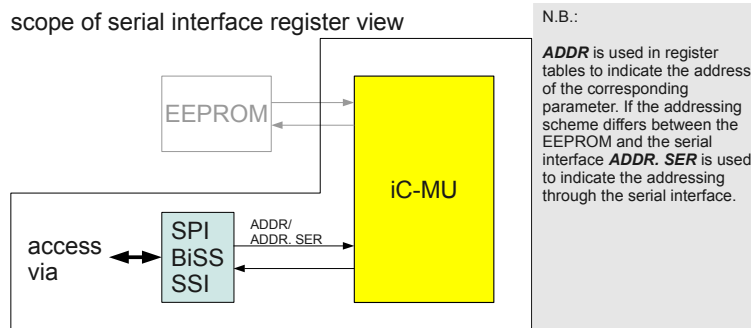


Figure 43: Scope of register mapping serial interface

The distribution of addresses in iC-MU corresponds to the document BiSS C Protocol Description which can be downloaded at [www.biss-interface.com](http://www.biss-interface.com).

The address translation for the addressable memory areas via the bank register to the EEPROM addresses is shown in Table 84.

iC-MU supports an addressing scheme using banks. Therefore the internal address space is divided into banks of 64 bytes each. The address sections visible via the I/O interface recognizes a "dynamic" section (addresses 0x00 to 0x3F) and a "static" section which is permanently visible (addresses 0x40 to 0x7F). The static address section is always visible independent of the bank currently selected. Figure 44 illustrates how the banks selected by BANKSEL are addressed.

Code	Description	Memory location during operation	Mode
CONF	0	internal register	iC-MU configuration data
EDS	1	E2P: 0x040-0x07F	<u>E</u> lectronic- <u>D</u> ata- <u>S</u> heet
	...	...	
	4	E2P: 0x100-0x13F	
USER	5	E2P: 0x140-0x17F	OEM data, free user area
	...	...	
	31	E2P: 0x7C0-0x7FF	

BANKSEL(4:0) Addr. SER:0x40; bit 4:0	
Code	Description
0x0	Selection of the memory bank
...	
0x1F	

Table 84: Address translation Addr Ser: 0x00-0x3F

Table 83: Register to select a memory bank

After startup the BANKSEL register ist set to 0.

The abbreviation *Addr. SER* used in the register tables of the specification of the iC-MU stands for the addressing of this register through the serial interface.

CONF: Bank 0, Addresses 0x00-0x3F								
Addr. SER	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	GC_M(1:0)		GF_M(5:0)					
0x01	GX_M(6:0)							
0x02	VOSS_M(6:0)							
0x03	VOSC_M(6:0)							
0x04	PH_M(6:0)							
0x05	ENAC				CIBM(3:0)			
0x06	GC_N(1:0)		GF_N(5:0)					

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CONF: Bank 0, Addresses 0x00-0x3F								
Addr. SER	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x07	GX_N(6:0)							
0x08	VOSS_N(6:0)							
0x09	VOSC_N(6:0)							
0x0A	PH_N(6:0)							
0x0B	MODEB(2:0)				MODEA(2:0)			
0x0C	CFGEW(7:0)							
0x0D	ACC_STAT	NCHK_CRC	NCHK_NON	ACRM_RES	EMTD(2:0)			
0x0E	ESSI_MT(1:0)		ROT_MT	LIN	FILT(2:0)			
0x0F	SPO_MT(3:0)				MPC(3:0)			
0x10	GET_MT	CHK_MT	SBL_MT(1:0)		MODE_MT(3:0)			
0x11	OUT_ZERO(2:0)			OUT_MSB(4:0)				
0x12	GSSI	RSSI	MODE_ST(1:0)		OUT_LSB(3:0)			
0x13	RESABZ(7:0)							
0x14	RESABZ(15:8)							
0x15	ROT	SS_AB(1:0)		ENIF_AUTO	FRQAB(2:0)			
0x16	LENZ(1:0)		CHYS_AB(1:0)	PP60UVW	INV_A	INV_B	INV_Z	
0x17	RPL(1:0)		PPUVW(5:0)					
0x18	TEST(7:0)							
0x19	RESERVED							
...								
0x1D	RESERVED							
0x1E	OFF_ABZ(3:0)				RESERVED			
0x1F	OFF_ABZ(11:4)							
0x20	OFF_POS*(19:12)							
0x21	OFF_POS*(27:20)							
0x22	OFF_POS*(35:28)							
0x23	OFF_COM**(3:0)				RESERVED			
0x24	OFF_COM**(11:4)							
0x25	PA0_CONF(7:0)							
0x26	RESERVED							
...								
0x3F	RESERVED							
Hinweis:	* OFF_ABZ value amended to include nonius/multiturn information							
	** OFF_UVW value amended to include nonius information							

Table 85: Register mapping bank 0, addresses 0x00-0x3F (access via serial interface)

OFF\_POS\* are the offset values (OFF\_ABZ) altered which are used as a start value for the counted internal cycle data. by the nonius calculation or by an external multiturn

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Static part: Addresses 0x40-0xBF									
Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x40				BANKSEL(4:0)					
0x41	EDSBANK(7:0)								
0x42	PROFILE_ID(7:0)								
0x43	PROFILE_ID(15:8)								
0x44	SERIAL(7:0)								
0x45	SERIAL(15:8)								
0x46	SERIAL(23:16)								
0x47	SERIAL(31:24)								
0x48	OFF_ABZ(19:12)								
0x49	OFF_ABZ(27:20)								
0x4A	OFF_ABZ(35:28)								
0x4B	OFF_UVW(3:0)				RESERVED				
0x4C	OFF_UVW(11:4)								
0x4D	PRES_POS(3:0)				RESERVED				
0x4E	PRES_POS(11:4)								
0x4F	PRES_POS(19:12)								
0x50	PRES_POS(27:20)								
0x51	PRES_POS(35:28)								
0x52	SPO_0(3:0)				SPO_BASE(3:0)				
0x53	SPO_2(3:0)				SPO_1(3:0)				
0x54	SPO_4(3:0)				SPO_3(3:0)				
0x55	SPO_6(3:0)				SPO_5(3:0)				
0x56	SPO_8(3:0)				SPO_7(3:0)				
0x57	SPO_10(3:0)				SPO_9(3:0)				
0x58	SPO_12(3:0)				SPO_11(3:0)				
0x59	SPO_14(3:0)				SPO_13(3:0)				
0x5A	RPL_RESET(7:0)								
0x5B	I2C_E2P_START(7:0)								
0x5C	I2C_RAM_START(7:0)								
0x5D	I2C_RAM_END(7:0)								
0x5E	I2C_DEVID(7:0)								
0x5F	I2C_RETRY(7:0)								
0x60	USER_EXCHANGE_REGISTERS								
...									
0x6F	RESERVED								
0x70									
0x71									
0x72	EVENT_COUNT(7:0)								
0x73									
0x74									
0x75	HARD_REV(7:0)								
0x76	CMD_MU(7:0)								
0x77	STATUS0(7:0)								
0x78	STATUS1(7:0)								
0x79	REVISION(7:0)								
0x7A	REVISION(15:8)								
0x7B	REVISION(23:16)								
0x7C	REVISION(31:24)								

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Static part: Addresses 0x40-0xBF								
Addr. SER	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x7C	REVISION(39:32)							
0x7D	REVISION(47:40)							
0x7E	MANUFACTURER(7:0)							
0x7F	MANUFACTURER(15:8)							
0x80	RESERVED							
...								
0xBF								

Table 86: Register mapping bank 0-31, addresses 0x40-0xBF (access via serial interface)

The current iC-MU hardware version can be read out through HARD\_REV.

HARD_REV(7:0) Addr. SER: 0x74; bit 7:0		
Code	Chip version	Addressing scheme using banks
0x02	iC-MU 0	-
0x03	iC-MU 1	-
0x04	iC-MU Z	-
0x05	iC-MU Y	x
0x06	iC-MU Y1	x

Table 87: HARD\_REV



## Address sections/Registerprotectionlevel

Register access can be restricted via RPL (see Table 88). RPL = 0x2/0x3 selects a shipping mode with limited access which can be set back to RPL = 0x0. To set back RPL the content of Bank: 0, Addr. SER: 0x17 has to be written to RPL\_RESET.

RPL(1:0) Addr. 0x17; bit 7:6		
Code	Mode	Access restriction
0x0	Configuration mode, no restrictions	RP0
0x1	Shipping mode, without command E2P_COM, reset is not possible	RP1
0x2	Shipping mode, with command E2P_COM, reset to RP0 possible	RP1
0x3	Shipping mode, without command E2P_COM, reset to RP0 possible	RP1

Table 88: Register access control

RPL_RESET(7:0) Addr. SER:0x5A; bit 7:0	
Code	Description
0x00	Set back value for RPL
...	
0xFF	

Table 89: Set back value for RPL

Sections CONF, EDS and USER are protected at different levels in shipping mode for read and write access (see Figure 44).

RPL(1:0) Addr. 0x17; bit 7:6			
RPL*	Section		
	CONF	EDS	USER
RP0	r/w	r/w	r/w
RP1	n/a	r	r/w
Note	*) RPL: Register Protection Level n/a: iC-MU refuses access to those register addresses r: Registers are readable w: Registers are writeable		

Table 90: Register Read/Write Protection Levels

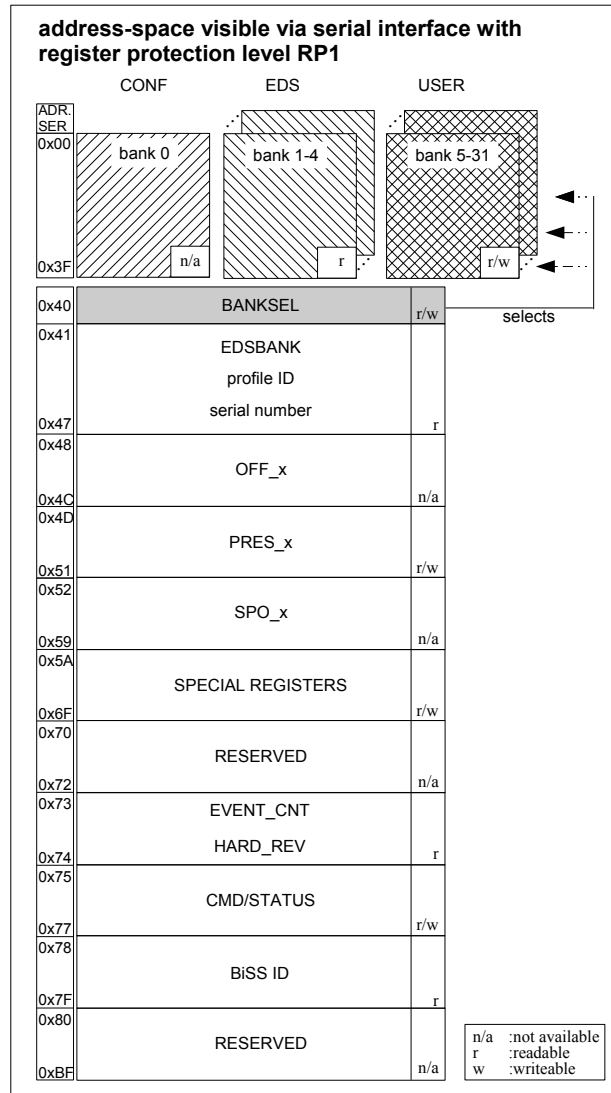


Figure 44: Principle of bank-wise memory addressing and access restrictions with register protection level RP1

## STATUS REGISTER AND ERROR MONITORING

### Status register

Various Status-information can be read out via status bytes STATUS0 and STATUS1.

STATUS0(7:0)		Addr. SER: 0x76; bit 7:0	R
Bit	Name	Description of status message	
4	STUP	Startup iC-MU	
3	AN_MAX	Signal error: clipping (nonius track)	
2	AN_MIN	Signal error: poor level (nonius track)	
1	AM_MAX	Signal error: clipping (master track)	
0	AM_MIN	Signal error: poor level (master track)	
	Notes	Error indication logic: 1 = true, 0 = false	

Table 91: Statusregister 0

STATUS1(7:0)		Addr. SER: 0x77; bit 7:0	R
Bit	Name	Description of status message	
7	CRC_ERR	Invalid check sum internal RAM	
6	EPR_ERR	Configuration error on startup: No EEPROM	
5	MT_ERR	Multiturn communication error	
4	MT_CTR	Multiturn data consistency error: counted multiturn ↔ external MT data	
3	NON_CTR	Period counter consistency error: counted period ↔ calculated Nonius position	
2	FRQ_ABZ	Excessive signal frequency for ABZ-converter	
1	FRQ_CNV	Excessive signal frequency for internal 12 Bit converter	
0	CMD_EXE	Command execution in progress	
	Notes	Error indication logic: 1 = true, 0 = false	

Table 92: Statusregister 1

ACC\_STAT configures, if the status registers show the actual or the accumulated status information.

If the accumulated status is configured, the status bits are maintained until the status register is read out or the command ABS\_RESET bzw. SOFT\_RESET are executed. This is valid except for EPR\_ERR, STUP and CMD\_EXE. These bits are set in the status register independent of the ACC\_STAT configuration while the status information is active. The status register can be accessed independently of the internal operating state.

ACC_STAT		Addr. 0x0D; bit 7
Code	Description	
0	Output of actual status information	
1	Output of accumulated status information	

Table 93: Output configuration of status register

### N.B.:

A read access to the reserved addresses SER: 0x3D and 0x3E also clears the accumulated status information STATUS0 and STATUS1 if ACC\_STAT is set to 1.

### Error and warning bit configuration

The output and the polarity of the error and warning bit within the different serial protocols (MODEA Table 28) can be found in Table 94. Messages are allocated to the error and warning bit by parameter CFGEW according to Table 95.

MODEA(2:0)		Addr. 0x0B; bit 2:0			
Function	Error		Warning		
	low active	high active	low active	high active	
SPI	-	-	-	-	
BiSS	x	-	x	-	
SSI	-	-	-	-	
SSI+ERRL	x	-	-	-	
SSI+ERRH	-	x	-	-	
ExtSSI	x	-	x	-	

Table 94: MODEA: error/warning-bit within serial protocols

CFGEW(7:0)		Addr. 0x0C; bit 7:0
Bit	Visibility for error bit	
7	MT_ERR/MT_CTR	
6	NON_CTR	
5	Ax_MAX und Ax_MIN	
4	EPR_ERR	
3	CRC_ERR	
2	CMD_EXE	
Bit	Visibility for warning bit	
1	FRQ_CNV/FRQ_ABZ	
0	Ax_MAX und Ax_MIN	
Notes	x = M, N Encoding: 0 = message enabled, 1 = message disabled	

Table 95: Error and warning bit configuration

If an error pin is configured using MODEB (Table 29), an internal error (see status register, ACC\_STAT configuration and error bit configuration with CFGEW) is signaled by the NER pin (PB3). The minimum message time for I/O pin NER can be set by EMTD.

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<b>EMTD(2:0)</b>		Addr. 0x0D; bit 2:0	
Code	min. disp. time	Code	min. disp. time
0x0	0 ms	0x4	50 ms
0x1	12.5 ms	0x5	62.5 ms
0x2	25 ms	0x6	75 ms
0x3	37.5 ms	0x7	87.5 ms

Table 96: Minimum error display time

## COMMAND REGISTER

### Implementing internal commands

An implemented command is executed depending on the written data value.

CMD_MU(7:0)		Addr. SER: 0x75; bit 7:0	W
Code	Command	Explanation	
0x01	WRITE_ALL	Write internal configuration and Offset values to EEPROM	
0x02	WRITE_OFF	Write internal Offset values to EEPROM	
0x03	ABS_RESET	Reset of Absolute value (including ABZ-part)	
0x04	NON_VER	Verification of actual position by doing a nonius calculation	
0x05	MT_RESET	New read in and synchronisation of multiturn value	
0x06	MT_VER	Read in of multiturn and verification of counted multiturn value	
0x07	SOFT_RESET	startup with read in of EEPROM	
0x08	SOFT_PRES	Set output to preset	
0x09	SOFT_E2P_PRES	Set output to preset and save offset values to EEPROM	
0x0A	E2P_COM	start EEPROM communication	
0x0B	EVENT_COUNT	increment event counter by 1	
0x0C	SWITCH	A variant of WRITE_ALL to write configurations of MODEA and RPL which inhibit register communications	
0x0D	CRC_VER	Verification of CRC16 and CRC8	
0x0E	CRC_CALC	Recalculate internal CRC16 and CRC8 values	
0x0F	SET_MTC	Set MTC-Pin *)	
0x10	RES_MTC	Reset MTC-Pin *)	
...0xFF	no function		
Note:	*) MODE_MT=0x00		

Table 97: Implemented commands

**WRITE\_ALL** stores the internal configuration and offset/preset values to the EEPROM. CRC16 and CRC8 are automatically updated.

**WRITE\_OFF** only stores the offset/preset data area to the EEPROM. CRC8 is automatically updated.

Command **ABS\_RESET** initiates a redefinition of the absolute value. A new nonius calculation is started.

If a multiturn is configured, this is read in and synchronized. Offset values OFF\_ABZ/OFF\_UVW are amended to include the cycle data and stored as OFF\_POS and OFF\_COM. The ABZ/UVW converter is restarted.

Command **NON\_VER** initiates a nonius calculation and the computed value is compared to the current counted period. If there is a discrepancy, error bit NON\_CTR is set in status register STATUS1.

With command **MT\_RESET** an external multiturn is read in anew and synchronized. Offset values OFF\_ABZ and OFF\_UVW are amended to include the multiturn data and stored as OFF\_POS and OFF\_COM. Attention: The ABZ/UVW converter is not restarted. If part of the multiturn data is used for the singleturn information, ABS\_RESET has to be executed instead.

With command **MT\_VER** an external multiturn is read in and the counted multiturn value is verified. If there is a discrepancy, error bit MT\_CTR is set in status register STATUS1.

With command **SOFT\_RESET** internal finite state machines and counters are reset. The EEPROM is read in anew. A redefinition of the absolute value is initiated (see **ABS\_RESET**)

Command **SOFT\_PRES** initiates a preset sequence (cf. page 56) with preset values PRES\_POS. The internal offset values OFF\_ABZ are changed to set the output value to the value given by PRES\_POS. The internal CRC8 is automatically updated.

Command **SOFT\_E2P\_PRES** initiates a preset sequence (cf. page 56) with preset values PRES\_POS. The altered offset values OFF\_ABZ are stored in the EEPROM. CRC8 is automatically updated.

Command **E2P\_COM** initiates communication with the EEPROM (RPL=0x00 and 0x02). Prior to this the following parameters must be configured:

- I2C\_DEVID
- I2C\_RAM\_START
- I2C\_RAM\_END
- I2C\_E2P\_START

The device ID is written to I2C\_DEVID (see Table 98). If an error occurs while communicating with an external EEPROM up to 3 new communication attempts are started by iC-MU.

I2C\_RAM\_START defines the start address in the internal RAM which in case of a

- write access: marks the begin of the data area that holds the data to be written
- read access: marks the begin of the data area where the data read from the EEPROM is written to

According to this I2C\_RAM\_END defines the end address of the data area in the internal RAM. The number of bytes NUM\_BYTES to be read/written are determined by the difference between I2C\_RAM\_END and I2C\_RAM\_START.

I2C\_E2P\_START defines the start address of the EEPROM from which NUM\_BYTES bytes should be read/written.

The USER\_EXCHANGE\_REGISTERS (see Table 86) can be used for the data-exchange with the EEPROM.

I2C_DEVID(7:0) Addr. SER:0x60; bit 7:0	
Code	Meaning
0xA0	write EEPROM
0xA1	read EEPROM

Table 98: I2C\_DEVID

I2C_RAM_START Addr. SER: 0x5E; bit 7:0	
Code	Description
0x00	I2C-RAM start address
...	
0xFF	

Table 99: I2C\_RAM\_START

I2C_RAM_END Addr. SER: 0x5F; bit 7:0	
Code	Description
0x00	I2C-RAM end address
...	
0xFF	

Table 100: I2C\_RAM\_END

I2C_E2P_START Addr. SER: 0x5D; bit 7:0	
Code	Description
0x00	I2C-EEPROM start address
...	
0xFF	

Table 101: I2C\_E2P\_START

With command **EVENT\_COUNT** the value of register EVENT\_COUNT is incremented by 1.

EVENT_COUNT(7:0) Addr. SER:0x73; bit 7:0	
Code	Description
0x0	Event counter
...	
0x1F	

Table 102: Event counter

The command **SWITCH** is a variant of the WRITE\_ALL command which makes it possible to write configurations of MODEA und RPL into the EEPROM which inhibit further register communications (e.g. MODEA=ABZ).

**N.B.:** RPL must be set to 0x0 before starting the command.

MODEA\_NEW and RPL\_NEW are used to set the target configuration of MODEA and RPL (e.g. ABZ, no RPL). On executing the command SWITCH MODEA and RPL are set to the target values and the configuration is written to the EEPROM. Finally MODEA and RPL are set back to the original values. This makes it possible to control the success of the EEPROM write process by reading STATUS1 (EPR\_ERR should not be set).

**N.B.:** CRC\_ERR is set after command execution if there is the cyclic CRC check configured by NCHK\_CRC=0 and the target values of MODEA and RPL differ from the originals values.

iC-MU starts with the interface and register protection level configured with MODEA\_NEW und RPL\_NEW after the next startup or after the execution of command SOFT\_RESET.

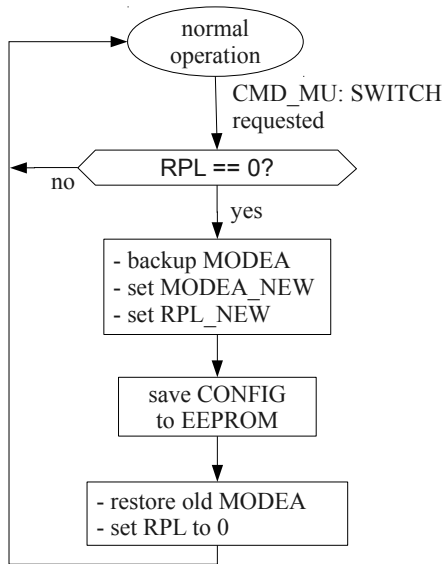


Figure 45: Event sequence of command SWITCH

MTD\_STATUS before it sets or resets pin MTC. To use these commands MODE\_MT has to be set to 0x0, i.e. no external multiturn is configured.

MTD_STATUS		Addr. SER: 0x60; bit 0
Code	Description	
0	MTD Pin was 0, before setting/resetting MTC	
1	MTD Pin was 1, before setting/resetting MTC	

Table 105: Status of pin MTD before command execution SET\_MTC and RES\_MTC

MODEA_NEW						Addr. SER: 0x60; bit 2:0
Code	PA0	PA1	PA2	PA3	Function	
0x0	NCS	SCLK	MOSI	MISO	SPI <sub>TRI</sub>	
0x1	NCS	SCLK	MOSI	MISO	SPI	
0x2	NPRES	MA	SLI	SLO	BiSS	
0x3	NPRES	A	B	Z	ABZ	
0x4	NPRES	MA	SLI	SLO	SSI	
0x5	NPRES	MA	SLI	SLO	SSI+ERRL	
0x6	NPRES	MA	SLI	SLO	SSI+ERRH	
0x7	NPRES	MA	SLI	SLO	ExtSSI	

Table 103: Target value of MODEA for the command SWITCH

RPL_NEW				Addr. SER: 0x60; bit 7:6
Code	Registerprotection	Command E2P_COM	Reset to RP0 possible	
0x0	RP0	x	x	
0x1	RP1	-	-	
0x2	RP1	x	x	
0x3	RP1	-	x	

Table 104: Target value for RPL for the command SWITCH

Command **CRC\_VER** starts a verification of CRC16 and CRC8. In case of an crc error, the CRC\_ERR status bit is set.

Command **CRC\_CALC** starts a recalculation of CRC16 and CRC8. CRC16 and CRC8 are saved internally in iC-MU and are used for later CRC verifications.

The command **SET\_MTC** sets pin MTC to logic level 1. **RES\_MTC** resets pin MTC to logic level 0. iC-MU saves the actual logic level of pin MTD to

## Configurable NPRES Pin

A configurable NPRES pin can be used at pin PA0 if MODEA is set to 0x2-0x7. This pin can be used to execute a command configured by PA0\_CONF on a falling edge of NPRES.

PA0_CONF(7:0)		Addr. 0x30; bit 7:0
PA0_CONF(7:0)		Addr. SER: 0x25; bit 7:0 Bank 0
Code	Command	
0x00	NO_FUNCTION	
0x01	WRITE_ALL	
0x02	WRITE_OFF	
0x03	ABS_RESET	
0x04	NON_VER	
0x05	MT_RESET	
0x06	MT_VER	
0x07	SOFT_RESET	
0x08	SOFT_PRES	
0x09	SOFT_E2P_PRES	
0x0A	E2P_COM	
0x0B	EVENT_COUNT	
0x0C	SWITCH	
0x0D	CRC_VER	
0x0E	CRC_CALC	
0x0F	SET_MTC	
0x10	RES_MTC	
...0xFF	no function	

Table 106: Command to be executed on falling edge of NPRES

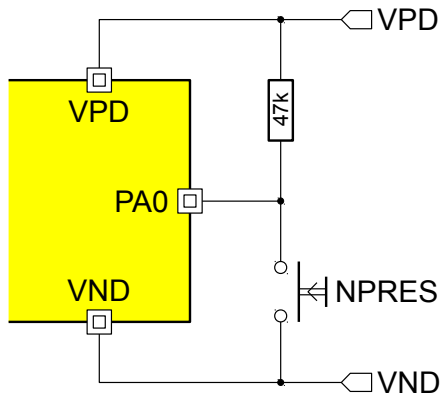


Figure 46: External circuitry for NPRES functionality

## POSITION OFFSET VALUES AND PRESET FUNCTION

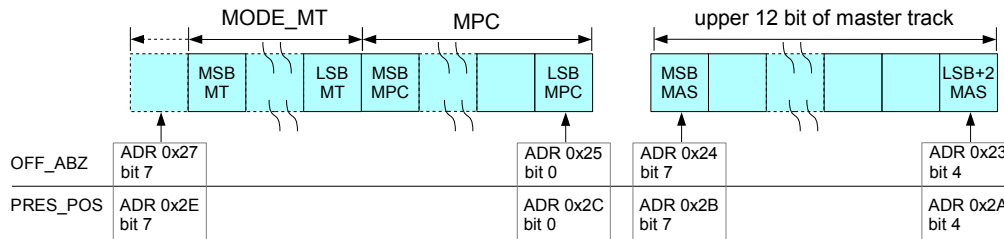


Figure 47: Position of the parameters OFF\_ABZ and PRES\_POS with respect to configured multiturn (MODE\_MT), periods (MPC) and converter resolution

OFF\_ABZ holds the position offset values stored in the EEPROM. After startup or the commands SOFT\_RESET and ABS\_RESET the OFF\_ABZ values are amended to include the nonius data and the multiturn data (in case an external multiturn is configured) and stored as OFF\_POS in the internal RAM. For output the OFF\_POS value is subtracted with each conversion from the internally synchronized result.

### Preset function

The preset function corrects the output position value of the ABZ, SPI, or BiSS interface to the setpoint given by PRES\_POS. Correction is initiated by writing command SOFT\_PRESET or SOFT\_E2P\_PRESET to the command register (see page 52), or, if one of these commands is configured with PA0\_CONF as NPRES command at PA0 pin, by a falling edge at NPRES. See Table 28 for configuration of NPRES and Table 106 for PA0\_CONF.

<b>OFF_ABZ(3:0)</b>	Addr. 0x23; bit 7:4	
<b>OFF_ABZ(11:4)</b>	Addr. 0x24; bit 7:0	
<b>OFF_ABZ(19:12)</b>	Addr. 0x25; bit 7:0	
<b>OFF_ABZ(27:20)</b>	Addr. 0x26; bit 7:0	
<b>OFF_ABZ(35:28)</b>	Addr. 0x27; bit 7:0	
<b>OFF_ABZ(3:0)</b>	Addr. SER:0x1E; bit 7:4	Bank0
<b>OFF_ABZ(11:4)</b>	Addr. SER:0x1F; bit 7:0	Bank0
<b>OFF_ABZ(19:12)</b>	Addr. SER:0x48; bit 7:0	
<b>OFF_ABZ(27:20)</b>	Addr. SER:0x49; bit 7:0	
<b>OFF_ABZ(35:28)</b>	Addr. SER:0x4A; bit 7:0	
Code	Description	
0x00000000	Offset position relative to absolute position	
...		
0xFFFFFFFF		

Table 107: Output offset position, relative to absolute position

<b>OFF_POS(19:12)</b>	Addr. SER:0x20; bit 7:0	Bank0, R
<b>OFF_POS(27:20)</b>	Addr. SER:0x21; bit 7:0	Bank0, R
<b>OFF_POS(35:28)</b>	Addr. SER:0x22; bit 7:0	Bank0, R
Code	Description	
0x00000000	Offset (is automatically computed)	
...		
0xFFFFFFFF		

Table 108: Output position offset amended by the nonius/MT

When the preset function is started, the ABZ converter is stopped. The current position is then determined. The correction factor for output (OFF\_POS) is calculated taking PRES\_POS into account and stored in the internal RAM. Offset values OFF\_ABZ are computed and if the command SOFT\_E2P\_PRESET is used written to the external EEPROM. The ABZ converter is then restarted.

<b>PRES_POS(3:0)</b>	Addr. 0x2A; bit 7:4
<b>PRES_POS(11:4)</b>	Addr. 0x2B; bit 7:0
<b>PRES_POS(19:12)</b>	Addr. 0x2C; bit 7:0
<b>PRES_POS(27:20)</b>	Addr. 0x2D; bit 7:0
<b>PRES_POS(35:28)</b>	Addr. 0x2E; bit 7:0
<b>PRES_POS(3:0)</b>	Addr. SER:0x4D; bit 7:4
<b>PRES_POS(11:4)</b>	Addr. SER:0x4E; bit 7:0
<b>PRES_POS(19:12)</b>	Addr. SER:0x4F; bit 7:0
<b>PRES_POS(27:20)</b>	Addr. SER:0x50; bit 7:0
<b>PRES_POS(35:28)</b>	Addr. SER:0x51; bit 7:0
Code	Description
0x00000000	Preset position
...	
0xFFFFFFFF	

Table 109: Output position preset



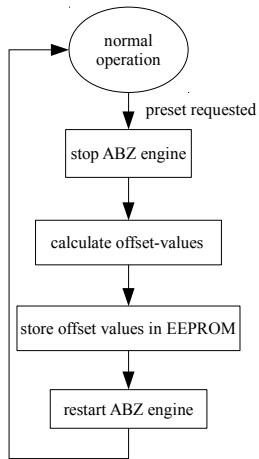


Figure 48: Preset sequence using command  
SOFT\_E2P\_PRES

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## DESIGN REVIEW: Notes On Chip Functions

iC-MU Z		
No.	Function, Parameter/Code	Description and Application Notes
		Please refer to datasheet release A3.

Table 110: Notes on chip functions regarding iC-MU chip release Z.

iC-MU Y1		
No.	Function, Parameter/Code	Description and Application Notes
1	CRC of output data iC-MU(2): IC operating mode BiSS or extended SSI (MODEA = 0x2, 0x7) and 3-track nonius with 4096 CPR (MPC = 12, OUT_LSB = 0x0)	Effects the construction of a multiturn system with two iC-MU (Page 40): 3-track nonius configuration with 2 iC-MU and 4096 periods, sensor data output using BiSS or extended SSI protocol (SSI with CRC) shows an invalid CRC. Data output according to the SSI or SPI protocol is not affected.

Table 111: Notes on chip functions regarding iC-MU chip release Y1

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# iC-MU OFF-AXIS NONIUS ENCODER WITH INTEGRATED HALL SENSORS

preliminary



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## ORDERING INFORMATION

Type	Package	Order Designation
iC-MU	16-pin DFN 5 x 5 mm	iC-MU DFN16-5x5

For technical support, information about prices and terms of delivery please contact:

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